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TDRSS MULTIMODE TRANSPONDER PROGRAM PHASE II - EQUIPMENT DEVELOPMENT

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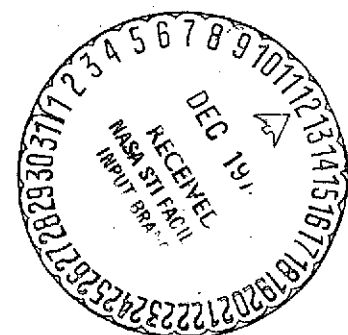
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PREFACE

This report, dated 15 October 1973, contains a description of the equipment designed during Phase I and fabricated during Phase II on a program entitled "TDRSS Multimode Transponder." The results of the Phase I study effort were previously published in a report designated "Magnavox Research Laboratories Report No. R-4403," dated 15 July 1973, and a description of the equipment which was subsequently developed during Phase II is presented in this report. This work was accomplished by the Magnavox Research Laboratories of Torrance, California, and complies with the requirements of Contract Number NAS5-20330.

Use of geosynchronous tracking and data relay satellites (TDRS) which can serve both low data rate users at VHF and high data rate users at other frequencies has been considered by NASA in recent years. The effects of radio frequency interference (RFI) from the earth and expected to pose problems for the TDRS system at VHF. Investigations have suggested several modulation techniques that offer promise to overcome these problems.

This report contains a complete description of the TDRS Multimode Transponder and its associated ground support equipment. The transponder will demonstrate candidate modulation techniques to provide the required information for the design of an eventual VHF/UHF transponder suitable for installation in a user satellite, capable of operating as part of a Tracking and Data Relay Satellite (TDRS) system.

Magnavox wishes to acknowledge the assistance of Pat Mitchell, NASA Technical Officer and Keith Fellerman of the TDRSS program office at the Goddard Space Flight Center.

This report was prepared by Messrs. R. Cnossen, J. Mackey, M. Wong, and D. Roberts of MRL; D. DeVito of ASAO, Magnavox; and V. Smith of Chu Associates.

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SECTION I

INTRODUCTION

1.1 PROGRAM BACKGROUND

To provide a virtual real time data acquisition and tracking capability, the TDRS system concept was developed by NASA. This capability would be used by low, medium, and high-data-rate users consisting of manned and unmanned scientific satellites. The TDRS system would provide the data acquisition and tracking capability for those manned and unmanned missions whose orbits were less than 5,000 kilometers.

Currently, unmanned scientific satellites are supported by the STDN (MSFN unified with STADAN) network consisting of ground stations strategically located on the globe. These stations are connected to a communications center, at the Goddard Space Flight Center, through NASCOM facilities. Manned missions are also supported by STDN. A second network, the Deep Space Network (DSN), also services NASA. The DSN, operated by JPL, services deep space exploration missions and can be used as backup for manned missions.

Subsequent to the initial Phase A study which established important TDRS concepts, NASA-Goddard contracted several detailed VHF link communications studies. Among these were: (1) the multipath modulation study conducted by Magnavox under contract NAS5-10744, (2) the multipath modulation study conducted by Hekimian Laboratories under contract NAS5-10749, and (3) the VHF communication study for low-data-rate users conducted by Hughes Aircraft under contract NAS5-11602. As a result, two prime candidate systems evolved. Pseudonoise modulation was recommended by Magnavox and Hughes while adaptive burst communications (ABC) was recommended by Hekimian. Hughes considered a narrowband forward link with a wideband return link, while Magnavox considered a narrowband PN forward link and options of either wideband or narrowband PN return links.

NASA issued to industry an RFP, dated May 1971, for a configuration and trade-off study of the TDRS system. Subsequently, two contractors, North American Rockwell and Hughes Aircraft, were awarded system trade-off studies. Next, NASA

issued an RFP for a multimode transponder to be used on board a low-data-rate, unmanned, scientific satellite. Shortly afterward this RFP was amended to permit the design of a multimode transponder for installation and use on board an aircraft simulating a user spacecraft as part of a TDRS system. On March 1, 1972, a contract (NAS5-20330) for the design and development of a multimode transponder was awarded to Magnavox Research Laboratories.

In June 1972, MRL presented to NASA the results of the Phase I portion of the Multimode Transponder development program. It included the system analysis used to identify hardware parameters, identified all known technical problems associated with hardware implementation and provided a complete multimode transponder design.

In September 1973, acceptance testing of the Multimode Transponder and its associated test equipment was successfully completed.

In October 1973, preliminary meetings were held to discuss modification of the Multimode Transponder to convert to S-band RF frequencies and to interface with an Adaptive Ground Implemented Phased Array system for system integration testing at the Applied Physics Laboratory of Johns Hopkins University.

1.2 BASIC TDRSS CONCEPTS

The forward and return links and the links between the proposed TDRS satellites and the ground station are illustrated in figure 1-1. One TDRS satellite is located at 14 degrees west and the other at 144 degrees west, resulting in a total separation of 130 degrees. The two TDRS satellites are active repeaters (amplifiers). The forward link is defined as the link from the ground station to TDRS to low-data-rate user: the return link is from user to TDRS to ground station. Forward user-TDRS links are on VHF or UHF frequencies and return user-TDRS links are on a VHF frequency. TDRS-ground station links are in the Ku band.

At the time the Multimode Transponder specification was finalized in July 1972, the user-to-TDRS link RF frequencies were assigned within the VHF/UHF region. The current thinking is that these link frequencies may be at S-band frequencies or even at Ku band frequencies instead. The ground station to TDRS link will be in the Ku band at 14.4 to 15.35 GHz. The TDRS-to-ground station link will be in the Ku band at 13.4 to 14.2 GHz.

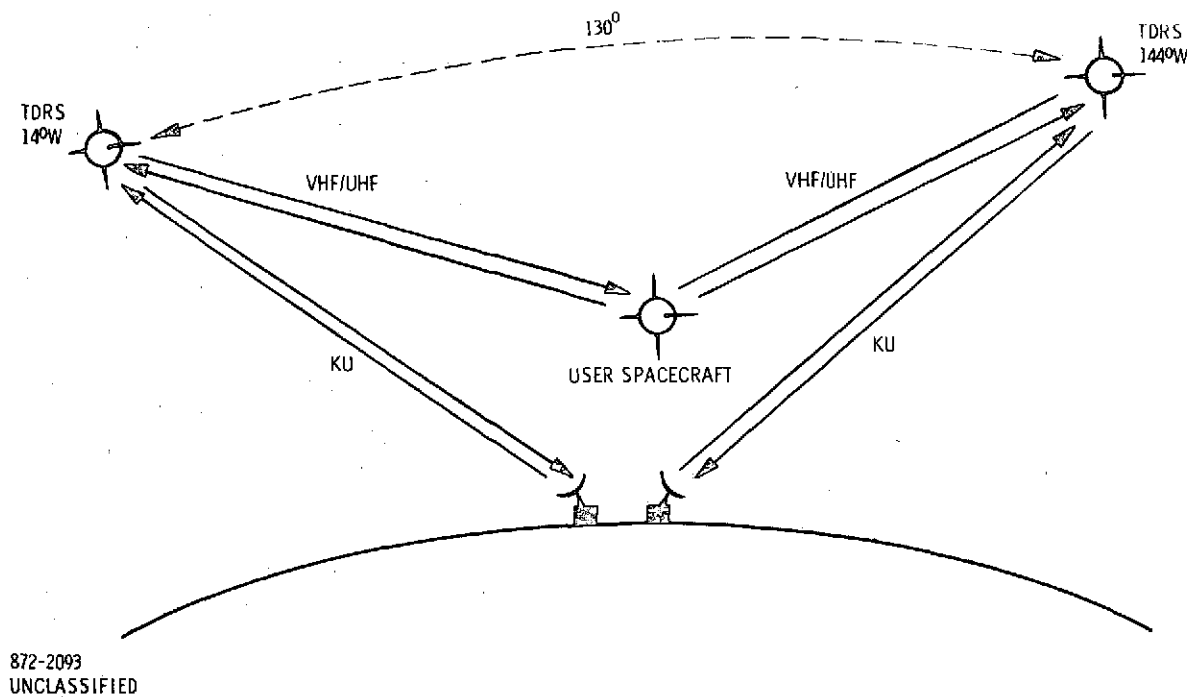


Figure 1-1. Simplified TDRS-User Geometry

Unmanned scientific satellites are required to dump accumulated data upon command as they pass over designated ground stations. Scientific data is accumulated on board by means of tape records and is transmitted to the appropriate ground station at greater than real time speed. The TDRS system will circumvent the need for on-board recorders by providing essentially real time data transfer and tracking commands for the low-data-rate users. During a single orbit, low-data-rate users can accumulate 5 to 6 megabits of data.

This data accumulation is based on a 100-minute orbit and a typical low-data-rate user. This means that a low-data-rate user, during a six-minute pass, would transmit recorded data to the ground station network at a rate of 15 to 20 kilobits per second. With the use of the TDRS system capability, this rate equated to a continuous rate of about 1 kilobit per second. The corresponding rate requirement for the forward link is to accommodate a command data rate of 100 to 1,000 bits per second.

In addition to providing forward and return link data transfers, the TDRS system must provide real-time tracking of range and range-rate measurements of the low data rate users. This can be accomplished through the use of one or two TDRS systems. Simultaneous tracking of a user with both TDRS systems is accomplished when the user is in the field of view of both TDRS systems.

Regardless of tracking techniques used, the range and doppler tracking uncertainty requirements below have been applied in the TDRS configuration.

- Systematic Range Errors

Less than 10 meters

- Random Range Errors

Less than 15 meters

- Doppler Uncertainties

Systematic 10 centimeters per second

- Random Range Rate Errors

10 centimeters per second for a doppler observation interval of one second or one centimeter per second for a doppler observation of 10 seconds.

Prior to the development of the Multimode Transponder, a number of TDRSS system concepts were established: The TDRS would be capable of transmitting a minimum of two simultaneous coded forward link signals for commanding user satellites. These two signals would provide command data, range and range rate data, and emergency voice. Each channel would have minimum EIRP of 30 dBw. This power level would be obtained over a circular field of view of not less than 26 degrees. This requirement meant that each TDRS system would be capable of transmitting two simultaneous channels of information. A user in the field of view of both TDRS systems would be capable of receiving and monitoring four channels, two from each TDRS system.

In the return link, 20 simultaneous accesses would be accommodated by each TDRS system. Although it was anticipated that more than 20 different low-data-rate satellites would be in orbit at any time, two low-data-rate accesses were anticipated for each TDRS system.

Although the TDRS system concept was straightforward, the problem areas below confronted system implementation:

- ⊙ Multipath
- ⊙ RFI
- ⊙ User antenna pattern anomalies
- ⊙ Multiple access of 20 users to a common repeater
- ⊙ Power output limitations inherent in the low-data-rate, unmanned, scientific satellites.

Multipath exists between the user and TDRS because it is anticipated that the unmanned users may not have stabilized antenna system capability but will be essentially omni-directional. Furthermore, satellite tumbling will create a time varying multipath situation. Multipath will exist in links from TDRS-to-user and from user-to-TDRS. In addition to additive noise at both the user and TDRS, RFI generated on the earth will serve to reduce system performance. The RFI can exist in both the forward and return links.

1.3 PROGRAM OBJECTIVES — PHASE II

The purpose of this effort was to provide NASA with a design and an engineering model of a VHF/UHF multimode transponder and its associated ground support equipment. The transponder will be capable of being installed aboard an aircraft which will demonstrate the modulation techniques specified herein. The multimode transponder will provide the required information for the design of a VHF/UHF transponder suitable for installation on a low altitude (5000 km or less) earth orbiting satellite, capable of operating as part of a Tracking and Data Relay Satellite (TDRS) system consisting of one or more geosynchronous satellites together with the associated ground equipment.

The transponder shall be designed for use on an aircraft simulating a low-altitude user satellite operating through a TDRS similar to ATS-F or to the GSFC Mark 1 and to its associated ground equipment. The transponder shall be designed, to the extent possible, to minimize weight, power consumption and cost. Reliability, shock and vibration specification shall be consistent with standard commercial specifications for aircraft flight equipment. Finally, the transponder shall be designed to meet all the electrical performance requirements of a space flight model, but not the packaging, reliability and space qualifications of a space flight model.

The Multimode Transponder (MMT), along with the associated ground support equipment (MTAR), will be designed to demonstrate the following modulation techniques:

- Conventional PSK command and telemetry mode
- Narrowband pseudorandom noise (PN) mode
- Wideband PN mode

The following functions will be simulated with various combinations of the transponder subunits and associated ground equipment:

- Reception, demodulation, and delivery to the user spacecraft of command signals received by the transponder via the forward link.
- Acceptance, modulation, and transmission via the return link of the telemetry data generated by the spacecraft user.
- Reception via forward link, processing on board, and retransmission via return link of coded signals suitable for ranging and range-rate determination.

1.4 REPORT CONTENT

Section I of this report contains the historical background for the TDRSS Multimode Transponder program and briefly outlines the objectives and tasks associated with the program.

Section II presents the TDRSS Multimode Transponder equipment configuration. It summarizes the modes of operation and provides a basic functional description of the equipment. A detailed description of the modes of operation and measurement techniques are also presented.

Section III contains a detailed functional description of the TDRSS Multimode Transponder design which consists of two major groupings of equipment; namely, the Multimode Transponder equipment (MMT) and the Multimode Transponder and Receiver equipment (MTAR). In addition, the MTAR antenna along with the test support equipment are separately described in detail.

Section IV provides a detailed mechanical description of all major assemblies. Each of these assemblies is shown pictorially and the construction techniques are illustrated in detail. Equipment capability with respect to environment and interface are discussed and size, weight and power specifications are included.

Section V presents the resulting equipment characteristics and performance. It includes the contract S.O.W. which has been modified to include all contract modifications. It describes the calculations used to determine the expected performance of the equipment. Finally, it includes the equipment characteristics measured during acceptance testing along with equipment performance data.

Section VI includes concluding remarks pertinent to the past, present and future of the Multimode Transponder equipment.

Section VII lists ways the equipment could be improved for future applications. It discusses the proposed S-band modifications and highly recommends a lab test program to evaluate and compare the many modes of operations.

SECTION II

SYSTEM DESCRIPTION

System concepts for the TDRSS Multimode Transponder equipment are described in this section. The terminal equipment configurations are shown, the various modes of operation are summarized, and a basic functional description is presented to provide insight to the system concepts which are presented in the latter portions of this report. This section also describes the operational procedures for the equipment and provides a rationale for many of the design features.

2.1 EQUIPMENT CONFIGURATION

2.1.1 MTAR EQUIPMENT

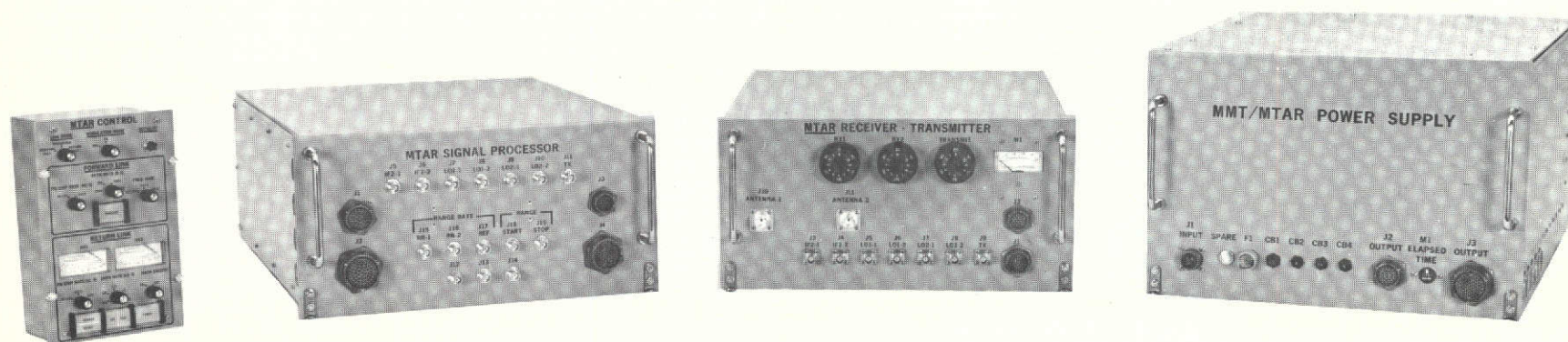
The complement of equipment which comprises the Multimode Transmitter and Receiver (MTAR) equipment is depicted in figure 2-1. This equipment performs the functions of transmit and receive equipment for an eventual TDRSS ground station. The MTAR equipment group consists of four major chassis: (1) Control-Display Panel, (2) Signal Processor, (3) Receiver-Transmitter and (4) Power Supply.

2.1.2 MMT EQUIPMENT

Figure 2-2 reveals the configuration of the Multimode Transponder (MMT) equipment. This group of equipment performs the functions of a transponder which will be part of an eventual TDRSS user transponder satellite. This equipment group consists of four major assemblies: (1) Power Supply, (2) Receiver-Transmitter, (3) Signal Processor and (4) Control-Display Panel.

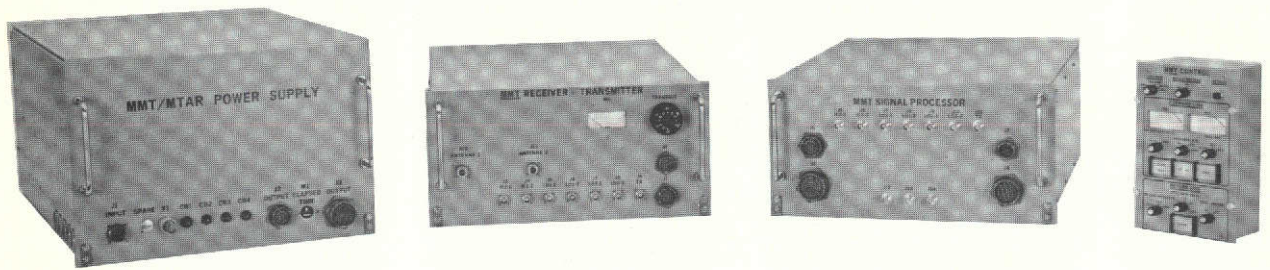
2.1.3 TEST SUPPORT EQUIPMENT

Comprising the test support equipment group is: (1) MX 270B Bit Error Rate Analyzer, and (2) MTAR/MMT Signal Monitor Box which includes a cable to interconnect with the signal processor assembly. This test support equipment, shown in figure 2-3, is supplied with both the MTAR and MMT equipment to: (1) generate and analyze data during performance testing, (2) interface audio equipment, and (3) monitor equipment status signals during experiments.



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Figure 2-1. Multimode Transmitter and Receiver (MTAR) Equipment



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Figure 2-2. Multimode Transponder (MMT) Equipment



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Figure 2-3. MTAR/MMT Test Support Equipment

2.1.4 INTEGRATED TEST CONFIGURATION

A method for interfacing and recording test data during laboratory experiments and flight tests is illustrated for the MTAR and MMT equipment in figures 2-4 and 2-5, respectively. The audio, data, data clocks and status data would be obtained from interface cable (J_1). The range and range rate signals would come from TNC coax connectors on the MTAR chassis. Data error pulses would come from a BNC connector on the MX 270 chassis. All of these signals would interface with NASA furnished recording equipment.

The audio signals would interface with a tape recorder and player. The accumulation of data error pulses would be counted with an event counter. The range and range rate signals would interface with time interval and frequency counters. All events would be coordinated with a time-of-day counter. All of this data including equipment status data would be stored in a data buffer and multiplexed into a Franklin printer for a permanent record.

2.2 MODES OF OPERATION

As the name implies, the multimode transponder has many modes of operation. The many equipment characteristics designed into the equipment are summarized in this section.

As shown in figure 2-6, there are five basic modes of operation:

- Data
- Encoded data
- Voice
- Range measurement
- Range rate measurement

Command and telemetry data may be transmitted and received via the forward and return links, respectively. In the return link, data may be encoded with a convolutional encoder with a constraint length of twenty three. PDM voice is provided for both forward and return links. Range and range rate measurement is available using a full transpond mode of operation.

As shown in figure 2-7, the MMT transmitter will operate at 137.0 MHz only and the MTAR will transmit at 127.750, 149 or 401 MHz. The multimode transponder has been designed to operate in the modulation modes shown in figure 2-8. Data rates selected on the basis of prior TDRSS studies are summarized in figure 2-9.

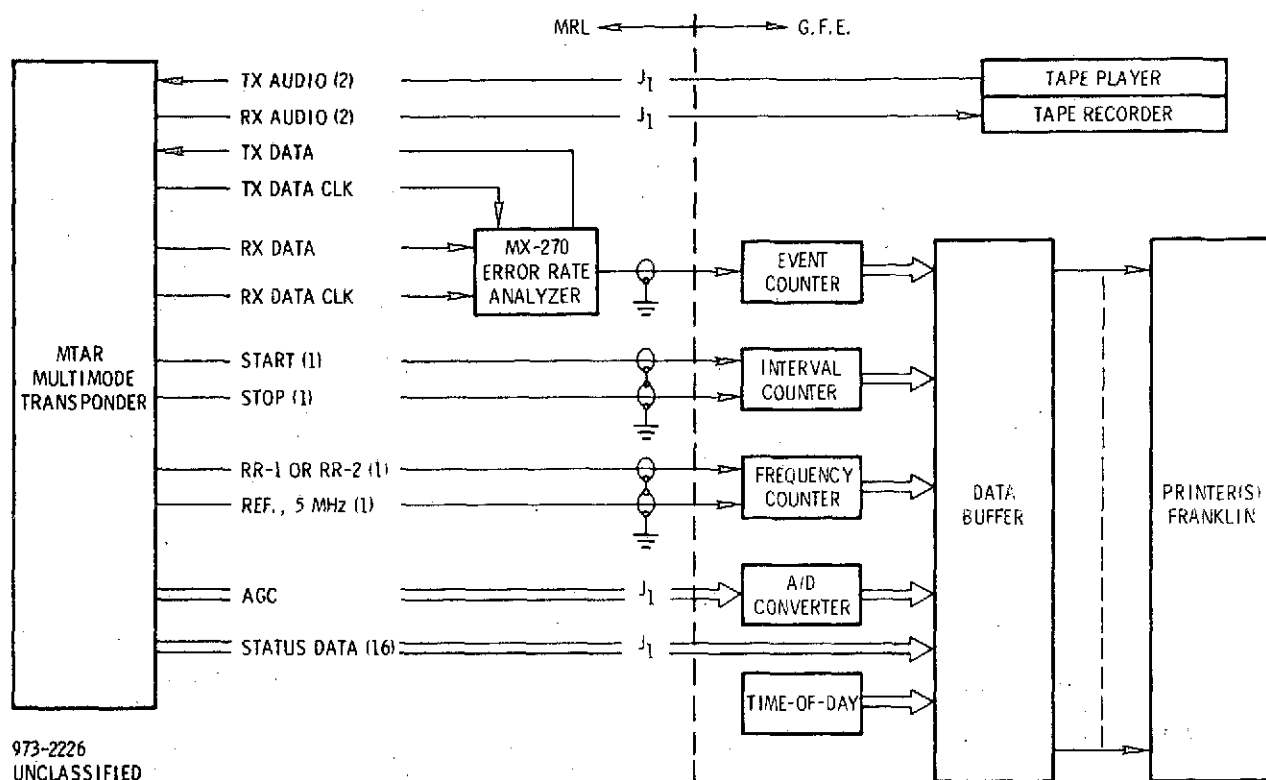


Figure 2-4. MTAR Flight Test Data Interface

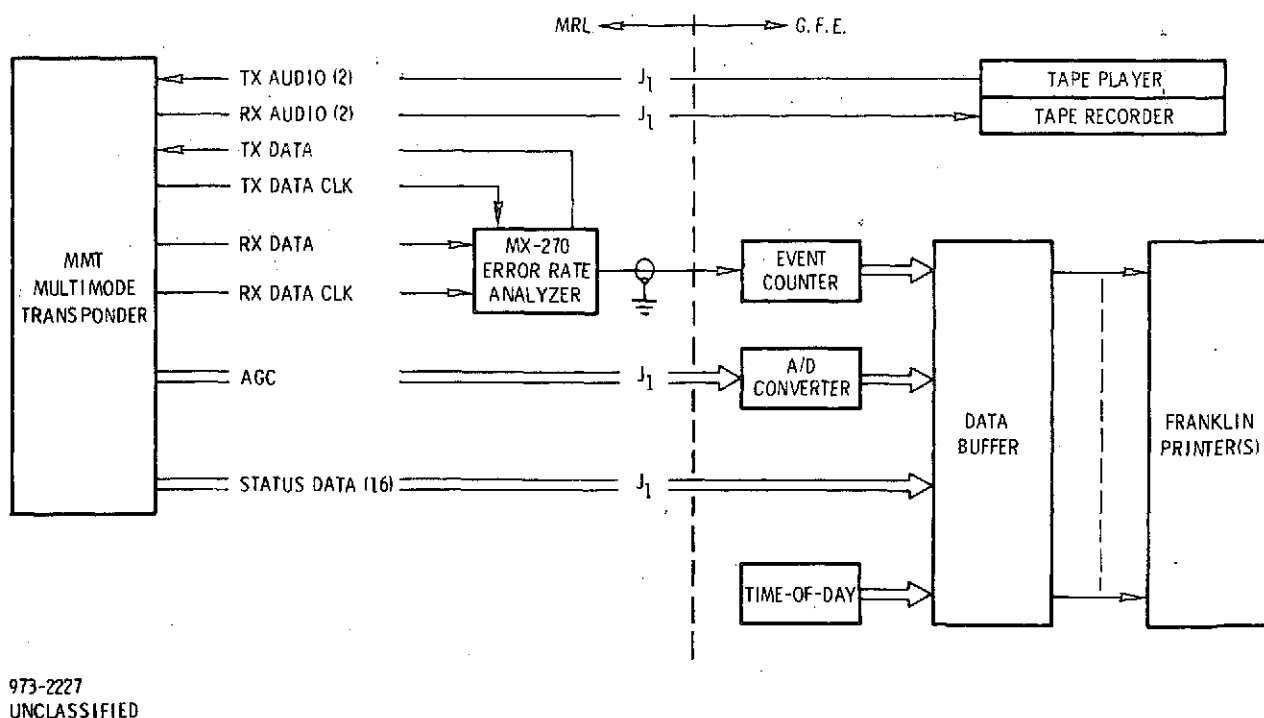


Figure 2-5. MMT Flight Test Data Interface

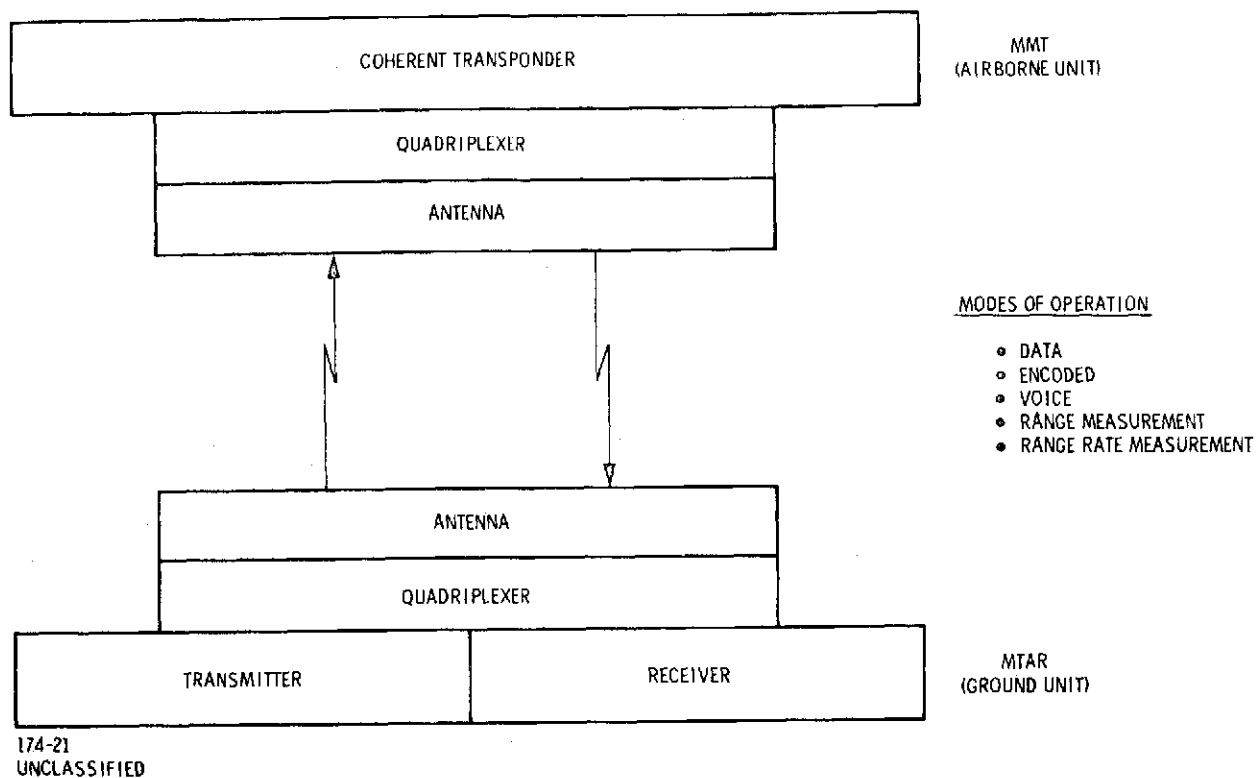


Figure 2-6. Modes of Operation

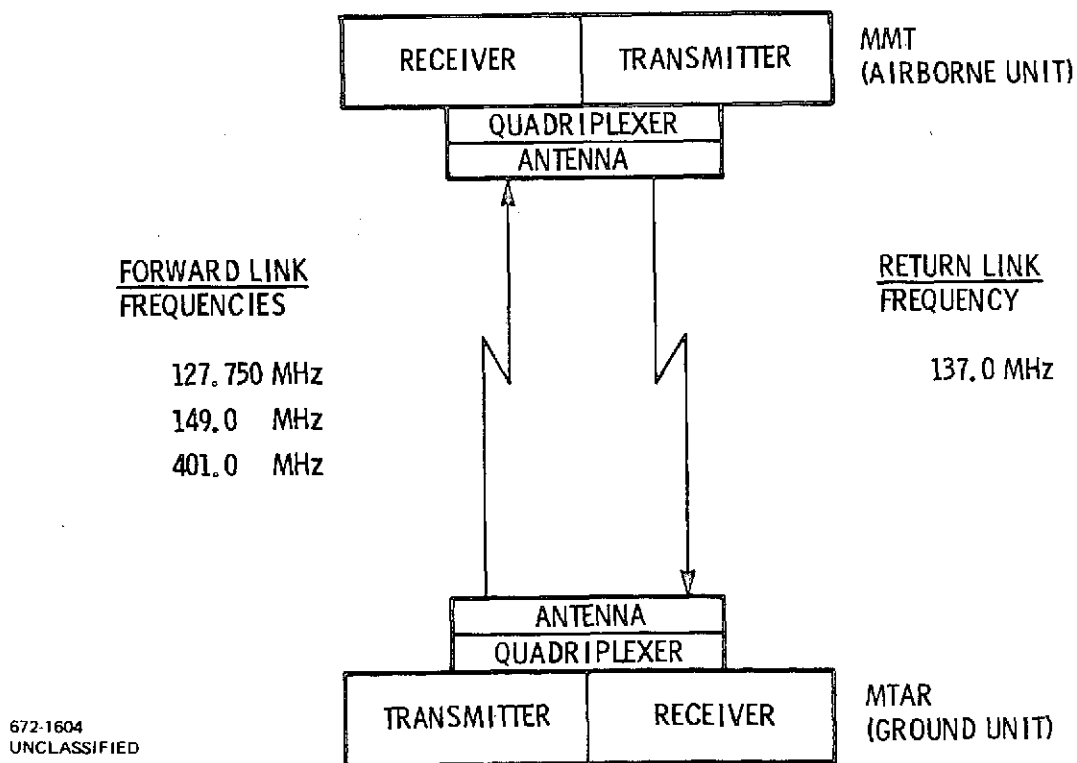


Figure 2-7. Selectable Frequencies

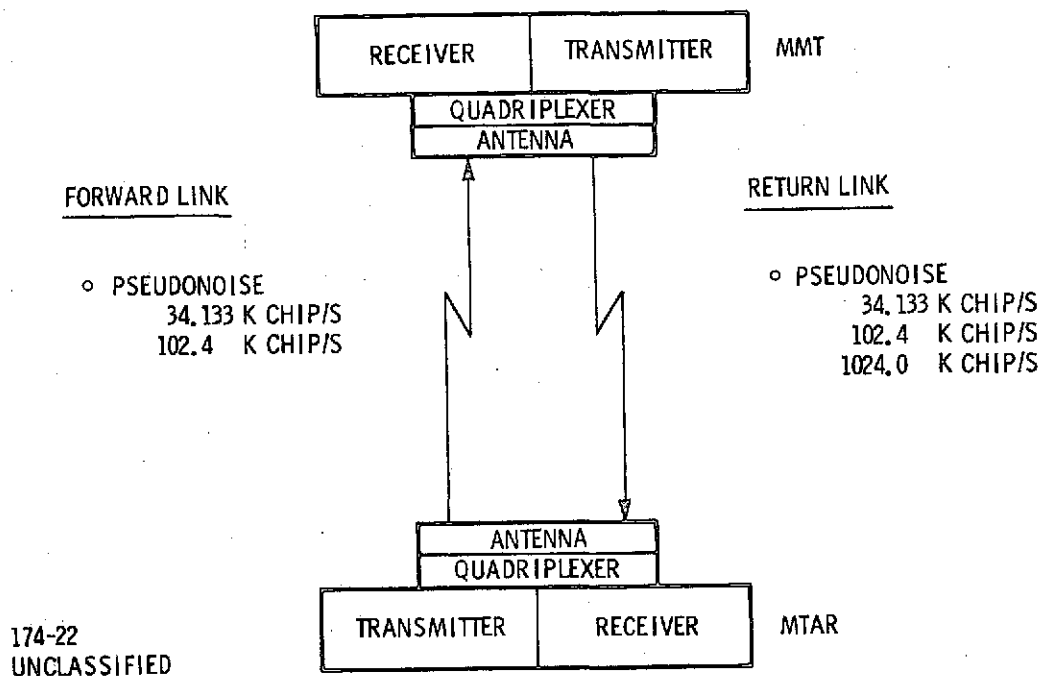


Figure 2-8. Modulation Modes

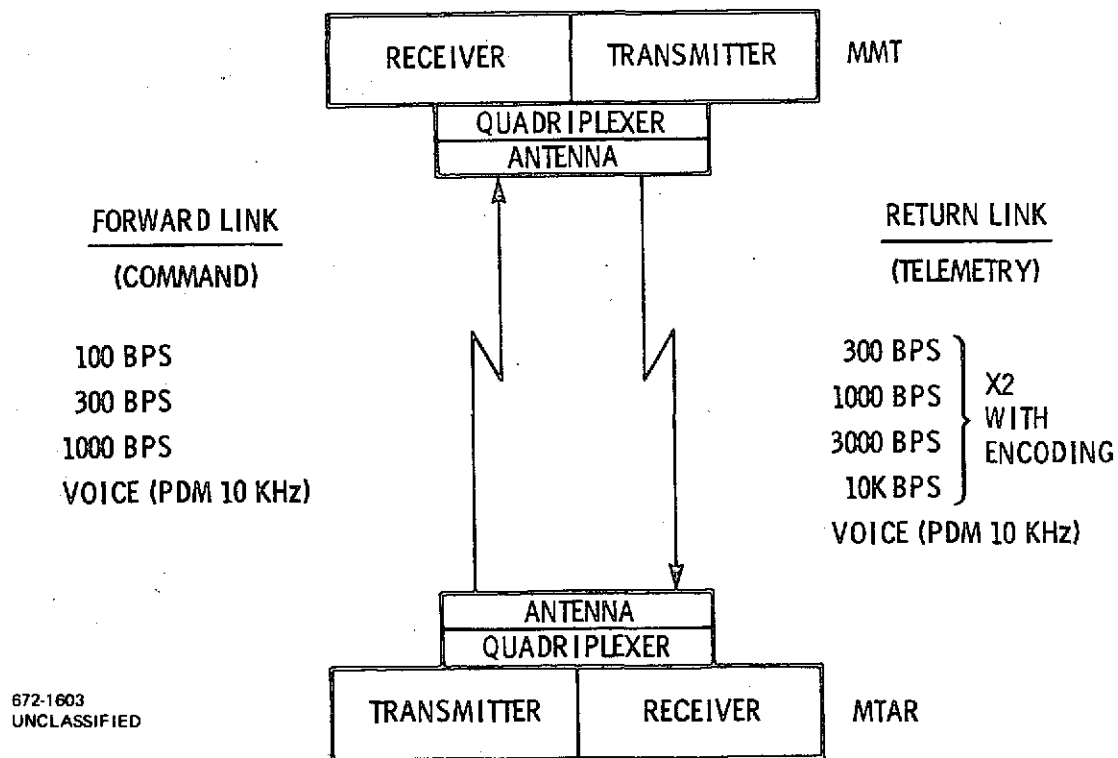


Figure 2-9. Data Rates

2.3 BASIC FUNCTIONAL DESCRIPTION

The roles and functional interactions of various subunits of the transponder during equipment operation in each of the above modes are described in the following paragraphs. The explanation of transponder circuit design will follow in section III.

The multimode transponder unit consists of two parallel receivers and a transmit channel as shown in the overall block diagram in figure 2-10.

The inputs for the two receivers are provided by orthogonally polarized antenna elements. The outputs of the two receivers are, after coherent detection, summed to provide a diversity combined output data signal. The receiver will operate in any one of three frequency bands: 127.750, 149 or 401 MHz.

In a similar manner, the transmitter is connected via quadriplexers to the polarization diversity antennas. However, in contrast to the receivers, which are always connected to their respective antennas, RF input to the transmitter is selected from the synthesizer of the receiver which is receiving with the highest signal-to-noise ratio. This procedure optimizes the coherent transponding signal radiation strategy. The transmitter will operate in one frequency band at 137 MHz.

The multimode transmitter and receiver (MTAR) consists of two parallel receivers and a single transmit channel which is shown in figure 2-11. The MTAR is very similar to the MMT; however, unlike the MMT which functions as a coherent transponder, the MTAR has a transmitter which functions independently from its two tracking receivers used for diversity. Another difference between the two equipments involves the external equipment interface.

2.3.1 CONVENTIONAL PSK MODE

In the conventional PSK mode the modulation technique is differential phase shift keying (DPSK) with a phase shift of ± 90 degrees. Essentially, this conventional mode is the basic, most fundamental mode of operation against which the performance of all other modes will be compared.

Briefly, the two signals, each derived from the separate diversity antenna, are coupled through the respective diplexers to the two separate receivers. In these receivers, the received signals are amplified and the ± 90 degree command modulation is recovered coherently by means of Costas-loop demodulation. Because the

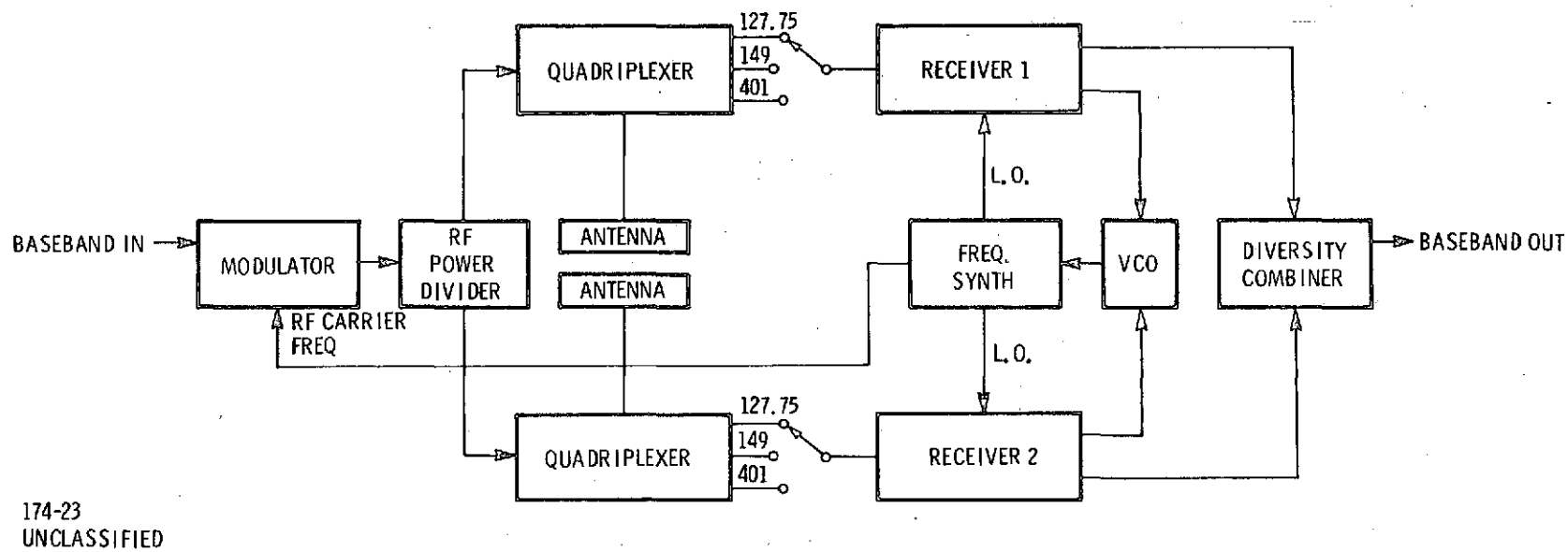
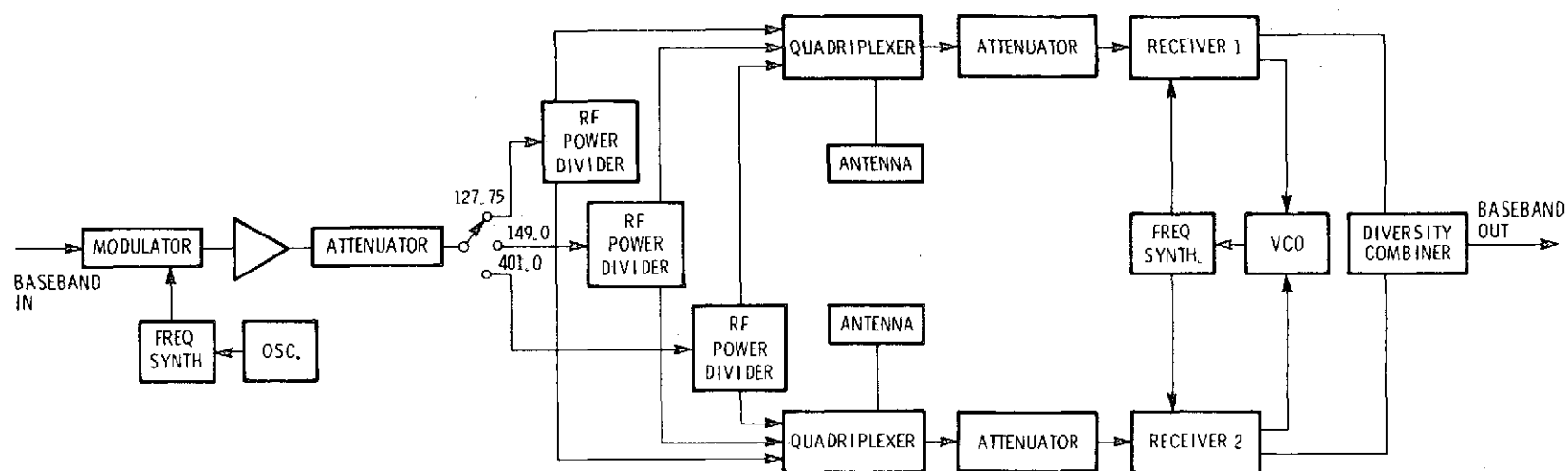


Figure 2-10. MMT Block Diagram



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Figure 2-11. MTAR Block Diagram

demodulators independently track the phase of each of the received carriers, the data recovery process is independent in each demodulator regardless of relative phase and frequency shifts between the two received carriers.

Separate voltage controlled oscillators (VCO), inside each receiver unit, track their respective carriers and provide the reference signals to their individual frequency synthesizers. These synthesizers provide both the local oscillator signals to their respective receivers. The transmitter carrier to the modulator and drive circuitry is selected from one of these synthesizers.

Because of the coherent tracking of the incoming carriers, each receiver portion of the transponder is simply a superheterodyne phase-locked loop tracking the received carrier (f_r) for coherent data demodulation. In phase lock,

$$f_r = N_1 f_o + f_o = (N_1 + 1) f_o$$

where f_o is the IF frequency and N_1 is the multiplication factor in the receive synthesizers. The transmit carrier frequency f_t is obtained in the synthesizers by multiplying f_o by N_2 , $f_t = N_2 f_o$, so that

$$\frac{f_r}{f_t} = \frac{N_1 + 1}{N_2}$$

which is the necessary condition for a coherent transponder. The constant N_2 is selected to yield an f_t of 137 MHz. Similarly, constant N_1 is selected to yield a local oscillator frequency required for the reception of one of the three selectable receive channels. The command data which appears at the outputs of the two respective in-phase demodulators, i.e., I-channel data No. 1 and No. 2, is applied to I channel combiner where the two data streams are combined according to a special diversity combining technique.

For transmission of telemetry data from a spacecraft to a ground station (return link), the transmitter modulators accept binary telemetry data and superimpose this data on one of two carriers selected according to the diversity strategy. In the conventional telemetry transmit mode, the modulation riding on the transmitter carriers is DPSK with phase modulation index of ± 90 degrees. The data rates are discrete 300, 1000, 3000 or 10,000 bps.

2.3.2 NARROW-BAND PN MODE

In the narrow-band PN mode, the forward commands and the return telemetry data is superimposed on PN binary codes clocked at rates consistent with a 50 kHz and 150 kHz channel bandwidth. Specifically, the chip rates are 34.133 or 102.4 kilochips per second, respectively.

The major additional subunits added to the transponder for this mode of operation are:

- Receiver coder
- Transmitter coder
- Code clock
- Search logic
- Code tracking loop

Briefly, in the PN mode, the receiver coder generates the PN code which, correlates with the received code after synchronization. Once the code is removed from the incoming signal the data is demodulated by means of a Costas loop. Initial search for the proper code phase is performed by search logic which is controlled by the doppler processor. Once code synchronism is established, the code tracking loop maintains it. Note that code tracking error is obtained by combining the outputs of the early-late tracking channels of both receivers. In this manner, code tracking will be maintained regardless of signal fading on either one of the channels.

After differential coding, the outgoing telemetry data is modulo-2 added to the transmit code and the combined binary stream modulates the transmit carrier. The selection of the transmitter drive signal is performed in the PN mode in the manner identical to the conventional mode.

The receive and transmit PN code chip rates are independently selected from the MMT control panel. However, these coders are driven from a common clock and the phases of the receive and transmit codes have a definite integral relationship.

2.3.3 WIDE-BAND PN MODE (RETURN LINK ONLY)

Transponder configuration in this mode is identical to the one in the narrow-band PN mode with the exception of the rate at which the transmitter coder is clocked after initial sync with narrow-band PN code. The chip rate for the

wide-band transmit mode is 1024 kilochips per second. Also, to provide for an extended code length, a special switching arrangement is used to extend the repetition period of the wideband code by a factor of 20. Since the receiver portion of the transponder is not modified when the wide-band transmission is used, the receive code tracking functions are the same as described in the preceding paragraph.

2.4 SYSTEM DESIGN

Rationale for the TDRSS Multimode Transponder System design is presented in this section. The concepts for the pertinent implementation techniques are described and many of the important operational sequences are summarized in the following discussions.

2.4.1 PSEUDONOISE TECHNIQUES

The advantages of pseudonoise communications and the reasons for each are summarized below.

- ⊙ Jamming protection is achieved because all unsynchronized signals are rejected owing to the narrow bandpass of the post-correlation circuits. Since the communicate codes are complex and can be changed at any time by the operator, the difficulty of recreating the spread-spectrum signal and achieving synchronization is apparent.

- ⊙ Message privacy is assured by modulating the baseband intelligence on the code rather than superimposing it directly on the carrier. The hostile monitoring station is thus required to break the code and synchronize in order to modulate the baseband data.

- ⊙ Low detectability of the spread-spectrum signal stems from the fact that its total power is distributed over a wide bandwidth, and the concentration of power at any given frequency over this band is far less than that normally associated with a conventional narrowband signal at the same frequency.

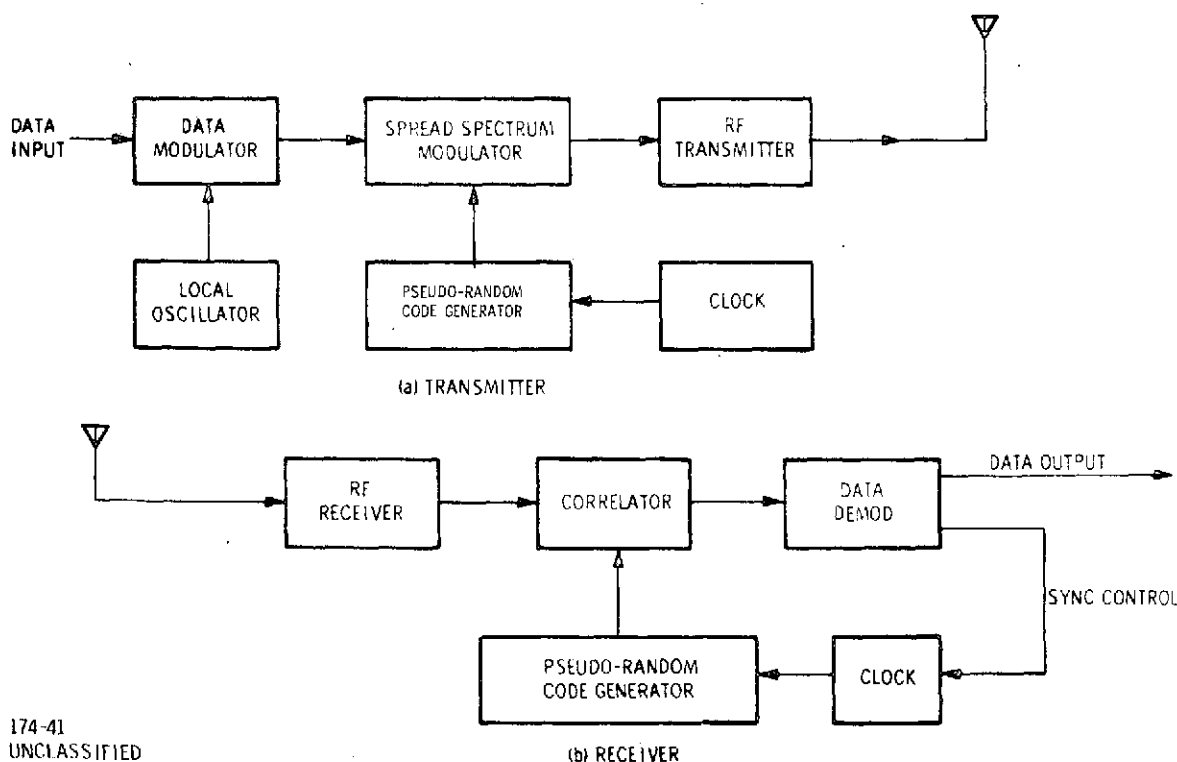
- ⊙ Multiple access is an inherent feature. Stations that share the same frequency channel can be called individually (and privately) by using orthogonal codes.

Basically, the pseudonoise wideband signal generated by the transponder is a double-sideband, suppressed-carrier signal centered at the selected RF frequency. This signal is produced by combining carrier with a digital pseudorandom modulating sequence, referred to as a code. The codes consist of various combina-

tion of "ones" and "zeros" which occur in what appears to be random order. The pseudorandom modulating voltage has characteristics similar to thermal noise; thus, the spread-spectrum signal is said to be pseudonoise-modulated. Despite its apparent randomness, the code possess a definite structure and is repetitvie over a long period of time. The pseudorandom-noise codes are not derived from a noise source but are generated by circuits in the modem.

Figure 2-12 shows the essentials of a pseudonoise system. In the transmitter, the data modulates a carrier in conventional fashion i.e., PSK for digital data. The resulting intelligence modulated carrier is then spread over a wide bandwidth by the pseudorandom code sequence from the code generator and amplified to rf.

If correlation occurs during the synchronization interval, the digital codes associated with the two signals are, in effect, cancelled, leaving a narrowband IF signal which contains only the subcarrier. The bandwidth of the post correlation demodulation circuits is just wide enough to accommodate this signal. If the locally generated code does not match the incoming signal, the power of the wideband received signal is spread over an even wider band. Thus, the received signal is rejected owing to the inconsequential power of the signal in the single narrowband slot.



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Figure 2-12. Block Diagram, Pseudonoise System

The receiving system accepts a particular pseudorandom-coded signal and rejects all others, thereby affording substantial jamming protection. This pseudorandom code sequence has a definite time length and is repetitive. The receiving system generates an rf signal modulated with a pseudorandom code identical to that of the received signal. The code of this local signal must be synchronized with the received signal to permit recovery of the modulation signal. The receiver searches for synchronization to determine whether the code being used to modulate the locally generated rf signal is identical to the code in the received signal. This search operation consists of comparing the two signals until correlation is recognized. The synchronization search procedure consists of reducing the frequency of the locally generated code slightly, causing the two signals being compared to undergo a constant displacement in phase. This is equivalent to sliding one coded rf signal past the other.

2.4.2 PN CODE SELECTION

The ability of a PN system to multiplex several users on the same frequency on a continuous basis depends on the orthogonality of the PN codes used. More specifically, the autocorrelation and cross correlation of the codes determine the multiple access interference and, consequently, the degradation to system ranging and data demodulation performance during multiple user operation.

The discussion which follows presents expressions for the autocorrelation function and cross correlation for a class of periodic PN codes which guarantee the maximum value of the cross correlation between codes of this class to be below a given bound. These codes are generally referred to as Gold codes. The derivation of cross correlation for integration window lengths less than the code length, i.e., partial correlation, is then presented, since in some cases the PN receiver will integrate over only part of the PN code and we might expect large values of cross correlation. Finally, the specific code selected for the Multimode Transponder and the technique used to implement it is presented.

2.4.2.1 Maximal Length Codes

If the feedback taps on an M stage shift register code generator are connected appropriately, a maximal length PN sequence will be generated. This

code has auto correlation properties defined by

$$\begin{aligned}
 R_{11}(\tau) &= \frac{\text{agreements} - \text{disagreements}}{\text{agreements} + \text{disagreements}} \\
 &= 1, \quad \tau = 0 \\
 &= -\frac{1}{2^m - 1}, \quad \tau \geq 1 \text{ chip}
 \end{aligned}$$

Since the cross correlation is a statistical quantity, we can postulate probabilistic models to describe it. Thus, we apply the binomial model to partial cross correlation and in using Gaussian approximation show that

$$\text{prob } |0| < k/w \sim N(k/\sqrt{w}) - N(-K/\sqrt{w}) \quad 1 < k \leq w$$

where

- 0 = cross correlation coefficient
- N = Gaussian distribution
- w = length of correlation window

This model is useful for correlation windows which are a small fraction of the code but it becomes poor for increasing correlation window length w , since the variance of the actual random variable approaches zero while the variance of the binomial model increases with increasing correlation window.

2.4.2.2 Gold Codes

Gold has shown that it is possible to select pairs of maximal length c codes which are generated from an m -stage register which have the following cross correlation properties,

$$\begin{aligned}
 R_{ij}(\tau) &= \frac{1}{2^{(m+2)/2} + 1} && m \text{ even} \\
 &= \frac{1}{2^{(m+1)/2} + 1} && m \text{ odd}
 \end{aligned}$$

The selection of these pairs results in an upper bound on the cross correlation between code pairs. Other codes selected from the family of maximals can produce very high cross correlation values.

2.4.2.3 PN Code Selected for the Multimode Transponder

The PN code selected for the Multimode Transponder is generated by a pair of 11-stage shift registers with feedback to generate a pair of maximal length codes that are combined to form the Gold code structure. The feedback taps for the two 11 stage generators are indicated by "ones" in the following sequences:

101 000 000 001
101 001 001 001

Described in octal format, the two PN sequences are:

5001 - α^2
5111 - α^3

A functional block diagram of the PN codes used to generate the codes described above is shown in figure 2-13.

The Gold code generator is useful because of the large number of codes it supplies while requiring only one pair of feedback tap sets. The Gold codes are generated by modulo-2 addition of a pair of maximal linear sequences. Every phase portion between the two maximal linear generation causes a new sequence to be generated.

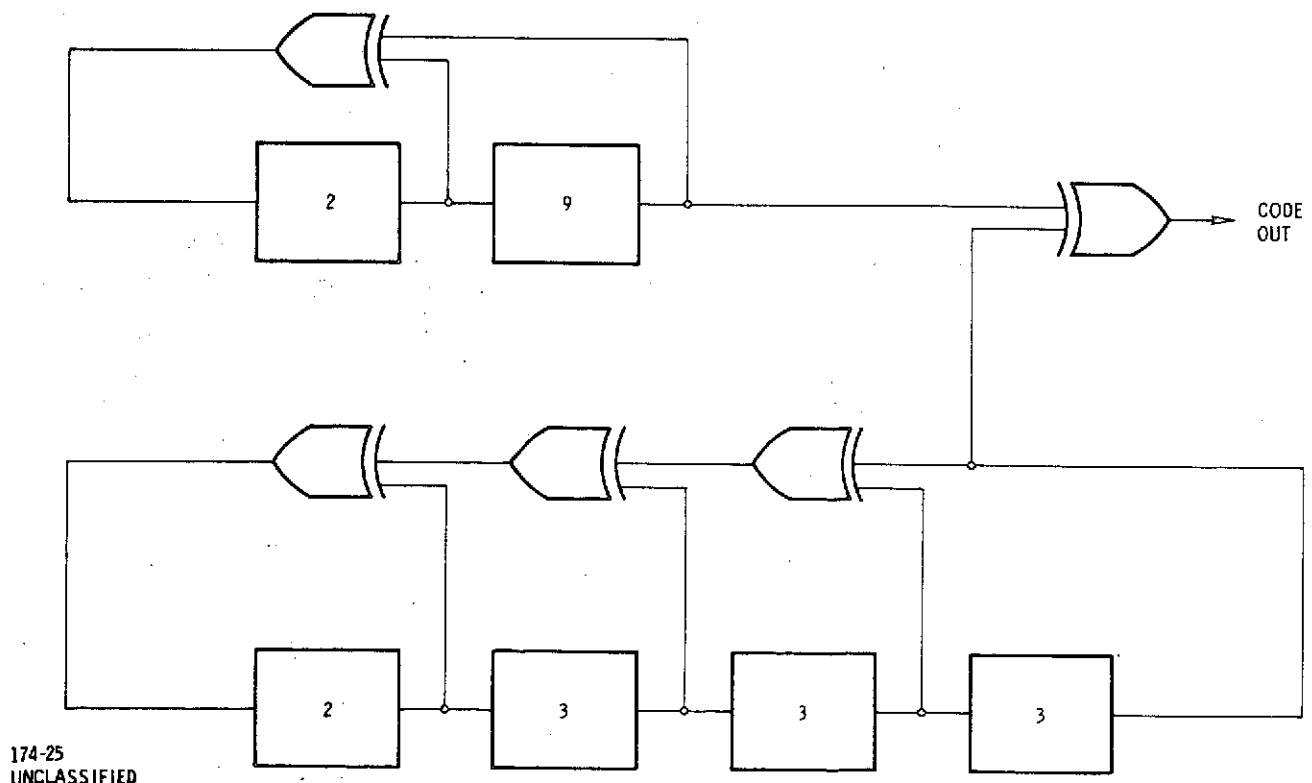


Figure 2-13. PN Coder

2.4.3 MULTIPLE ACCESS CAPABILITY

Provisions for an extensive multiple access capability inevitably lead to some degradation of the performance of a wideband system. Considerations of the primary factors of (1) maximum and most probable numbers of simultaneous accesses together with (2) the ease of implementation, permitted selection of a simple effective technique for multiple access accomplishment. The selected technique is quasi-orthogonal multiplexing (QOM). As used here, this technique is effective at a central terminal in discrimination of various remote addressors.

The QOM technique employs the total allotted RF bandwidth for multiple simultaneous access. Discrimination is accomplished by PN code characteristics only, i.e., an addressee will attain code correlation only with a transmission PN coded with an identical sequence. Thus the noise level (where noise is taken to include the uncorrelated transmissions to or from other users) seen by any receiver is somewhat increased but analysis indicates this disadvantage to be insignificant with the limitation of user satellites. The effect is further reduced by the selection of quasi-orthogonal codes for minimization of mutual interference.

The QOM technique for multiple access requires, as a practical matter, near equal signal strength of all transmissions in order to permit the addressee to discriminate adequately. The return link is not identical; ranges, user to TDRS is a non-limiting, linear repeater. Thus, a greater variation of received signal powers will be apparent at the ground station in a possible final configuration. However, analysis of expected geometries and of other variables indicates that degradation of discriminatory capabilities by the ground complex is relatively insignificant.

Following is an abbreviated analysis of MA capabilities of the QOM technique. It considers first the multipath interference encountered and subsequently considers interference due to other uncorrelated signals.

2.4.3.1 Interference Due to Multipath

The multipath medium is represented by the differential time delay structure where the zero delay and unity gain path is the direct one, and all other paths correspond to resolvable multipaths having a delay τ_m and a time-varying vector gain \hat{a}_m . The characteristic of each path is actually a time-varying random variable, with the average interval of stationary corresponding to the differential Doppler, or

fade rate, for that path. The receiver output $Y(t)$ consists of the transmitted signal $X(t)$ which is received on the direct path plus M multipaths, plus additive noise $N(t)$, and the additive interference of L random accesses which are each received via similar but independent multipath structures. The expression for Shannon capacity in this situation is

$$C = [W] \max \left[\log \frac{1}{2_{1-\rho^2}} \right]$$

W = system bandwidth

ρ^2 = normalized crosscorrelation between $X(t)$ and $Y(t)$

$$\rho^2 = \frac{\langle X(t) Y(t + \tau) \rangle^2}{\langle X^2(t) \rangle \langle Y^2(t) \rangle}$$

Now the crosscorrelation between $X(t)$ and the output of each multipath is zero. This is due both to the fact that the minimum multipath delay is greater than a PN chip width (the PN correlation function goes to a negligible value for this case), and the fact that the random time variation of the characteristic of each path will give a zero average crosscorrelation. The crosscorrelation of $X(t)$ and the noise and the other multiple access terms of course also is zero. Only the direct path contributes to the numerator of ρ^2 . However all the multipaths and the other factors constitute interference power and thus contributes to the denominator of ρ^2 . One then gets the following result for the crosscorrelation.

$$\rho^2 = \frac{S_i^2}{[S_i][S_i + A_m S_i + N_i + LA_L (1 + A_m) S_i]}$$

S_i = desired received signal power on direct path

A_m = relative power level of all the multipaths

A_L = average relative power level of each interfering access

L = total number of interfering accesses

$N_i = N_o W$ = receiver noise power in bandwidth W .

Therefore

$$S/N_o = \frac{1}{\frac{n_o}{E_b} + n a_L (1 + a_m)}$$

$$n = \frac{1}{a_L (1 + a_m)} \left[\frac{1}{S/N_{o \text{ req'd}}} - \frac{1}{E_b/n_o} \right]$$

for PN, non-coded data

For a noncoded, PSK modulated digital data signal, the $S/N_{o \text{ req'd}}$ is about 10 dB for a 10^{-5} bit error rate. Using this value, bandwidth efficiency versus power efficiency for the case of equal strength access and equal strength multipath is indicated in figure 2-14. For other cases of relative multipath strength, and/or relative access strength, one merely scales the ordinate n by the values of these relative strengths.

2.4.3.2 Interference from Other Users

For the case of coded data modulation of the PN carrier, the above expression still applies, but now one uses the smaller value of $S/N_{o \text{ req'd}}$ that is achievable with coding to obtain improved performance. For an optimized rate

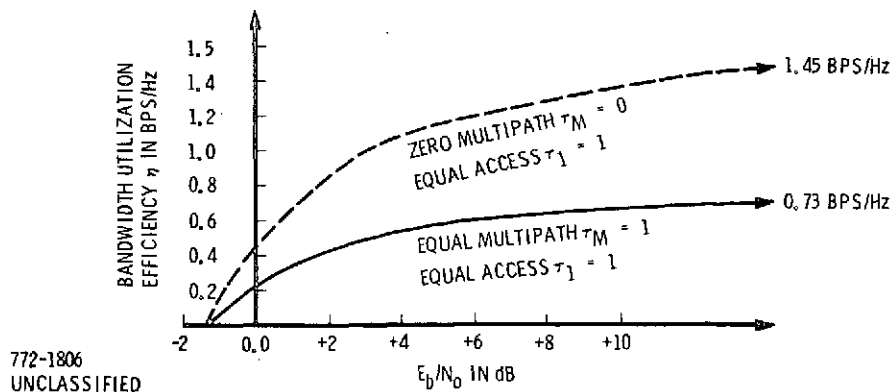


Figure 2-14. Bandwidth Efficiency vs. Power Efficiency for PN

1/2 sequential decoding, and a bit detection error rate of 10^{-5} , an $S/N_{\text{req'd}}$ per bit of 5.5 dB is achievable with hard decisions, whereas 4.5 dB is achievable with soft decisions.

For the case of PDM voice modulation of the PN carrier, the form of the above expression also still applies, except that now n must be interpreted as the product of the number of accesses times the PDM bandwidth (or clock rate) all divided by the PN bandwidth (or chip rate). Also the appropriate $S/N_{\text{req'd}}$ of 0 dB (threshold) or 10 dB (good quality) must be used.

Based on those limits and on pre-established power, bandwidth and geometric relationships capabilities are adequate for the expected maximum number of required accesses.

2.4.4 SEARCH STRATEGY FOR MULTIPATH

To provide a practical and implementable acquisition scheme for the multimode transponder which would be compatible with the current TDRS concepts and at the same time provide a reasonable link acquisition time (<40 sec.), several assumptions were made:

- In a normal mission TDRS handover will occur within 20 degrees of the horizon. (Figure 2-15 indicates the geometry)
- Multipath energy for a 5000 Km orbit is approximately 12 dB lower than for a 300 Km orbit.
- Diffuse multipath is not stable and will not cause false lock.
- The relative power contained in the specular component of multipath is reduced about 15 dB at high grazing angles.

Since a multipath signal is always time delayed with respect to the true signal, the strategy for preventing lock to a multipath signal would be to advance the code phase in excess of the worst case multipath (≈ 40 ms) upon first detecting the presence of a signal and resume search until the local code correlates with the real direct path signal.

Figure 2-16 indicates multipath time delay for various values of the angle θ as shown for multipath geometry in figure 2-15.

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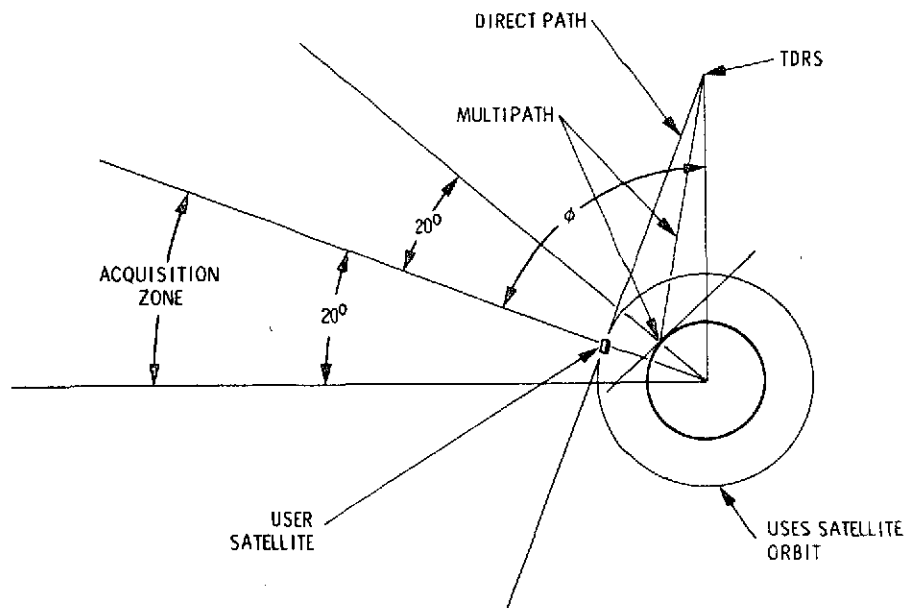


Figure 2-15. Multipath Geometry

The strategy selected for multipath rejection during a PN acquisition mode is to shift the local PN code phase backward in time in 1/2 chip steps. Upon detecting the presence of a signal, the code phase is advanced approximately 2 ms and backward search is resumed until correlation has been achieved a second time. This two-step procedure disallows acquisition to a multipath signal within 20° of the horizon, since multipath signals in this region are always delayed 2 ms or less as shown in figure 2-17.

During a PN track mode, multipath signals will be rejected because the minimum code length will be 40 ms which is longer than the greatest multipath delay in the TDRS configuration.

Details of the PN acquisition strategy in the presence of multipath are shown in figure 2-17. Two cases are illustrated: The first is where the local PN replica of the receiver is between the arriving signal and the multipath signal. The second case is where the local signal is ahead of the arriving and multipath signals.

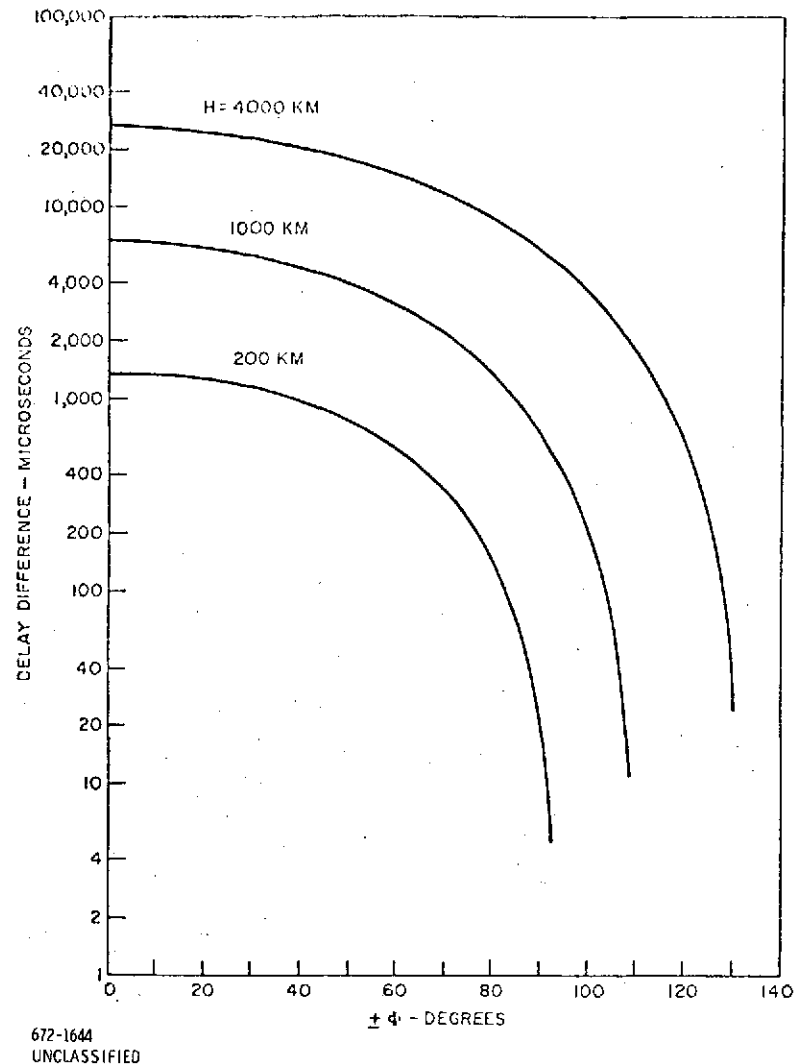
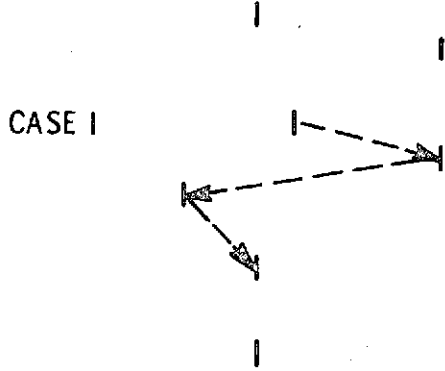
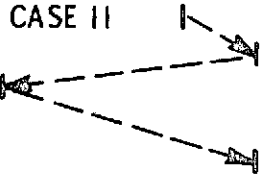


Figure 2-16. Multipath Time Delay

2.4.5 PN ACQUISITION TIME

For given orbit conditions, it is possible to readily compute limit conditions for (1) multipath delay time, and (2) doppler rates. The PN code length is selected to equal the maximum multipath delay time and its chip rate is determined by the width of the channel allocation. PN acquisition is governed by code characteristics including length and chip rate and is a relatively straightforward operation.

Large doppler ranges such as those characterizing TDRS add certain complexities to the acquisition process. Presence of unpredictable extreme dopplers requires a search throughout the total frequency range for acquisition. The two search

ADVANCE \leftarrow CODE PHASE \rightarrow RETARD	TIME	CODE	COMMENT
CASE I 	$t_0 - t_3$ $t_0 - t_3$	ARRIVING MULTIPATH	SEARCH MODE SIGNAL ALARM 2 mS RETRACE THEN RESUME SEARCH SIGNAL VERIFY
	t_0 t_1 t_2	LOCAL LOCAL LOCAL	
	t_3	LOCAL	
	$t_0 - t_3$ $t_0 - t_3$	ARRIVING MULTIPATH	
CASE II 	t_0 t_1 t_2	LOCAL LOCAL LOCAL	SEARCH MODE SIGNAL ALARM 2 mS RETRACE THEN RESUME SEARCH SIGNAL VERIFY
	t_3	LOCAL	
	$t_0 - t_3$ $t_0 - t_3$	ARRIVING MULTIPATH	
	t_0 t_1 t_2	LOCAL LOCAL LOCAL	

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Figure 2-17. Acquisition Strategy in the Presence of Multipath

parameters are (a) frequency positioning and (b) code positioning. The requirements for PN acquisition is dependent on satisfactory accomplishment of both of those searches. The choice of techniques for accomplishment of this complete search is of considerable importance in reduction of acquisition time.

The selected technique (see Section 2.4.6) utilizes a novel approach for search time reduction. The technique employs what is, in effect, a spectrum analyzer operating over the full band of doppler uncertainty. In conjunction with that device, a technique for sequential stepping of the code position is employed. In use, the code is held in a given position while the total possible doppler range of carrier frequencies is searched in suitable increments. In succession, this sequence is repeated with the code shifted one half chip at a time. This sequence is continued until an increase of signal strength at baseband indicates that the correct combination of code position and frequency has been attained. Certain confirmatory techniques are employed to assure that the signal is (1) valid and (2) not due to multipath, and following that, affirmation suitable adjustments are made to permit continued lock to the incoming signal.

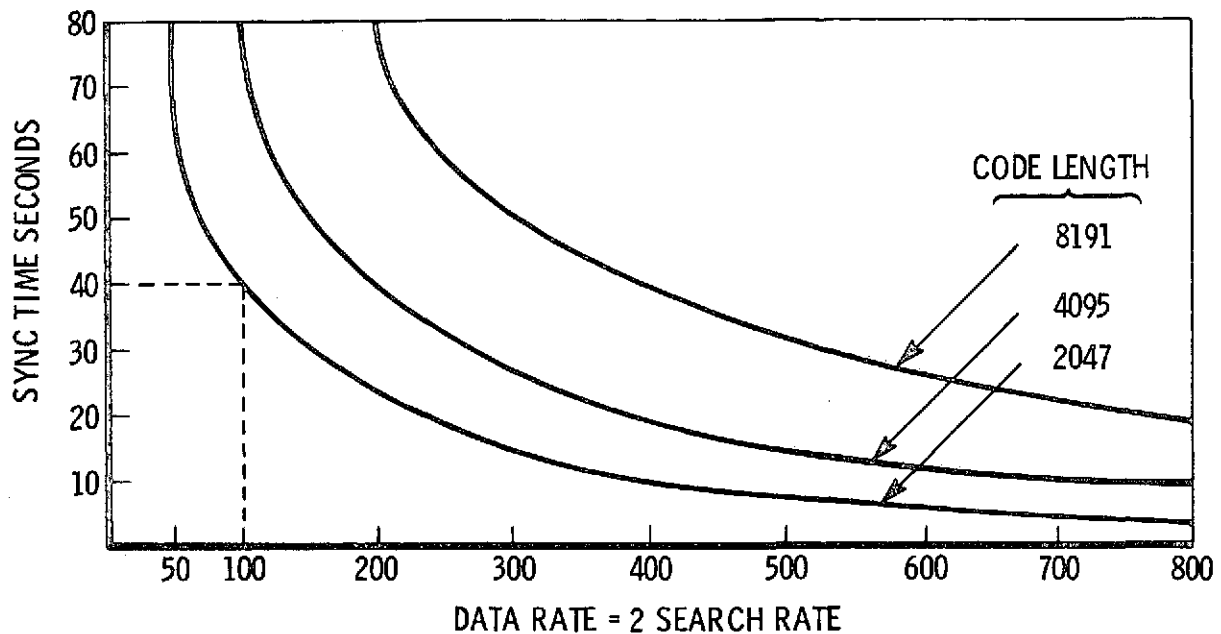
The unique and time saving feature of the acquisition system lies in the use of digital techniques for storage of signal strength data over the total range of doppler uncertainty. These data are stored in a memory which is searched for frequency position at a high rate for each 1/2 chip increment of code position. While this search is in progress a second identical memory is being filled with updated information and is subsequently employed for search at the next 1/2 chip increment of code. The first memory is erased during that period and refilled with current data. The two memories are continuously alternated. Time saving results from the great increase in speed of reading the digital memory as compared to an analog measurement.

The use of diversity channels also affects acquisition time. In the current mechanization the PN acquisition time is doubled when diversity is employed. Essentially, this results from the existence of only one set of hardware for acquisition as described. Representative PN acquisition times for selected situations are shown in Table 2-1.

Table 2-1. Average PN Acquisition Times for Representative Link Parameters

PN Code Chip Rate K Chips/ Sec.	Carrier Frequency MHz	Data Rate BPS	Signal Threshold C/N ₀ , dB	Doppler Range KHz	Average Acquisition Sec.
34	127.750	100	30	4	25.0
34	401	1000	40	12	2.5
102	127.750	100	30	4	50.0
102	401	1000	40	12	5.0

The indicated acquisition times are for a non-diversity situation. The acquisition time is devoted to searching all possible combinations of doppler shift and code chip position and in confirmation of the correctness of preliminary lock-on indication. It should be noted that the doppler search increments are 100 Hz wide in the low data rate modes indicating while at the high data rate the doppler search increments are 1000 Hz in width, thus decreasing the doppler shift search time even though the higher PN chip rate increases the time of code synchronization search, the net result being a shorter total acquisition time. Figure 2-18 presents acquisition time versus data rate for three code lengths.



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Figure 2-18. Acquisition Time vs Data Rate

Alternative approaches for rapid acquisition are available for implementation. Typical are:

- Permit the employment of a priori knowledge of the user satellite position and rate. Use of this information should permit a radical reduction of the doppler uncertainty. That reduction should be reflected in a near-directly-related reduction of acquisition time.

- Employment of greater EIRP of the TDRS will reduce the "false alarm" rate and result in acquisition time reduction.

2.4.6 DOPPLER RESOLVER

It is well known that the optimum detector for a CW pulse of known frequency in Gaussian noise is a matched filter. When the frequency is known only within some range, the best strategy is to employ a number of matched filters, one for each

resolvable frequency in the range. A practical digital implementation using this technique was used for mechanization of the doppler resolver. The block diagram in figure 2-19 illustrates the mechanization.

If the frequency is known, a classical matched filter is optimum for enhancing the signal-to-noise ratio when the signal is accompanied by additive Gaussian noise, prior to envelope detection and decision. By "known" is meant that product of the pulse duration, T , and the frequency uncertainty, W , is less than 1. If the product is on the order of 1, or a little more, then without much loss in the quality of detection, the matched filter may be segmented so that it effectively integrates over n intervals T/n seconds long, such that $WT/n \gg 1$. Each segment is detected and the n detected values are then added. Thus, some postdetection integration is used in place of predetection integration. As n gets large the process becomes increasingly inefficient. For example, when $n = 100$, the loss relative to ideal predetection integration (the matched filter) is on the order of 4 to 6 dB.

The superior approach is to provide a set of matched filters, one for each frequency across the uncertainty region at intervals of about $1/T$ Hz. Thus, the number of filters required is on the order of WT .

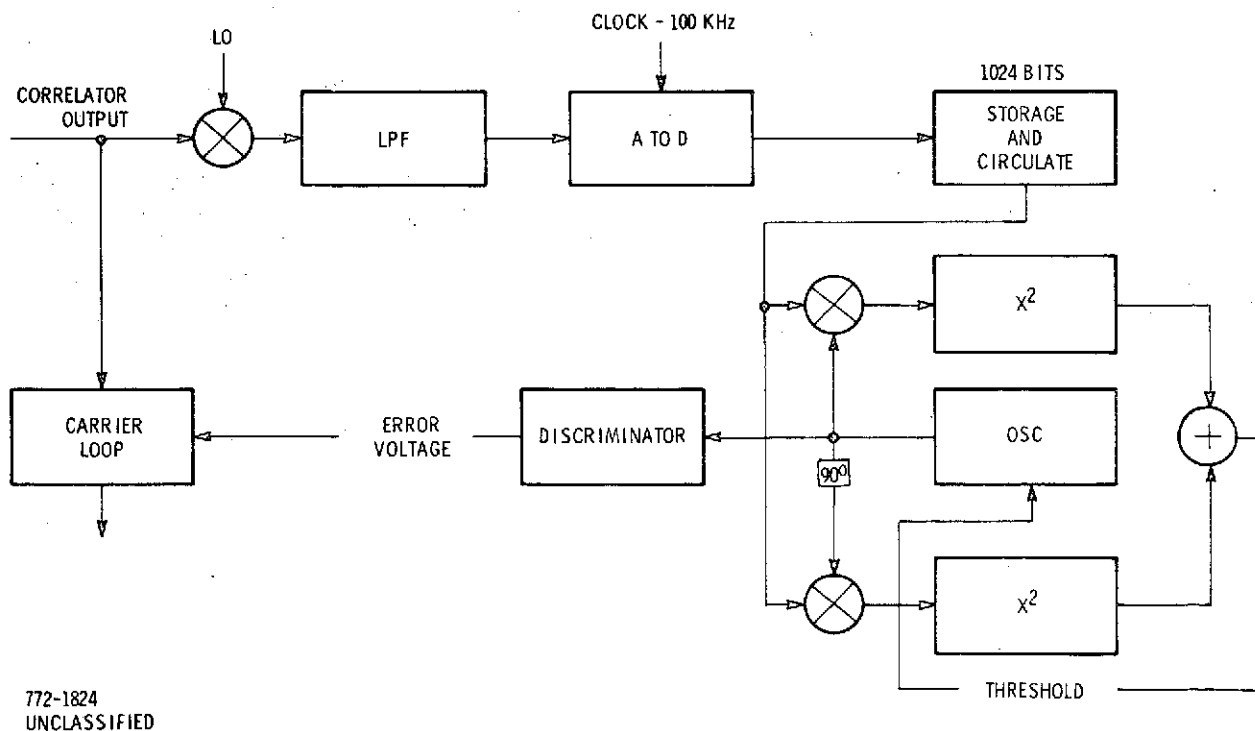


Figure 2-19. Doppler Resolver Block Diagram

The pulse of unknown frequency can be represented as

$$P(t) = A \cos [(\omega_c + \omega_a)t + \theta] \quad 0 < t < T$$

where ω_c is the nominal center frequency and ω_a is unknown, uniformly probable over the range $\pm 2\pi W$. Assume WT to be an integer, M ; if necessary by over-estimating W slightly.

The first step in the process is to bandpass filter the signal-plus-noise using a filter of bandwidth $2W$ centered at $\omega_c/2\pi$ Hz. The principal operation next performed is the computation of the Fourier coefficients of the filtered signal-plus-noise on the interval $(0, T)$. In particular, it is desired to compute the power in each component corresponding to frequencies in the filter passband. These quantities are the values of C_u^2 where

$$C_u = \frac{1}{T} \int_0^T f(t) \exp(-j2\pi n/T) dt$$

for values of n in the region $\frac{\omega_c T}{2\pi} \pm WT$.

Alternatively, C_u^2 can be obtained

$$C_u^2 = a_n^2 + b_n^2$$

where

$$a_n = \frac{1}{T} \int_0^T f(t) \cos 2\pi nt/T dt$$

$$b_n = \frac{1}{T} \int_0^T f(t) \sin 2\pi nt/T dt$$

In the mechanization it is necessary to store $f(t)$ (which is $P(t) + \text{noise}$) at the filter output. This is conveniently done by resolving $f(t)$ into its quadrature

components, sampling and quantizing so that digital memory can be used. The quadrature components of $f(t)$ with respect to a carrier at ω_c are $f_c(t)$ and $f_s(t)$ such that

$$f(t) = f_c(t) \cos \omega_c t + f_s(t) \sin \omega_c t$$

where

$$f_c(t) = A \cos (\omega_a t + \theta) + n_c(t)$$

$$f_s(t) = -A \sin (\omega_a t + \theta) + n_s(t)$$

in which n_c and n_s are independent Gaussian noise processes of zero mean, the same power, both bandlimited to the frequency interval $(-W, +W)$. On the basis of sampling theory, it would be adequate to sample f_c and f_s at the rate of $2W$ samples per second, however, as a practical matter sampling should be at $3W$ to $4W$ samples per second to allow for nonideal filtering and to improve the accuracy of the numerical approximations to the integrals. Call the actual sampling rate R , such that RT is a convenient integer. Amplitude quantization of the samples can be performed as crudely as one bit, however, this entails a loss of nearly 2 dB in output signal-to-noise. The use of 3 bit (8 level) quantization reduces this loss to a few tenths of a dB. The sampled, quantized values of $f_c(t)$ and $f_s(t)$ will be represented by $F_c(m/R)$ and $F_s(m/R)$ where the range of the integer m is 1 to RT corresponding to the range of $t: 0 < t \leq T$.

Before writing a final expression for a_n and b_n , it is useful to note certain symmetries in the expressions for values of n spaced equally above and below the midband value, $\omega_c T/2\pi$. To make these evident, let $n = k_c + k$ where $k_c = \omega_c T/2\pi$. The range of k which is of interest is $\pm WT$. Making these changes in notation, approximating $f_c(t)$ and $f_s(t)$ by their sampled, quantized counterparts, and approximating the integrals by sums, we obtain:

$$a_{\pm k} = \frac{1}{2RT} \sum_{m=1}^{RT} F_c\left(\frac{m}{R}\right) \cos \frac{2\pi k m}{RT} \mp \frac{1}{2RT} \sum_{m=1}^{RT} F_s\left(\frac{m}{R}\right) \sin \frac{2\pi k m}{RT}$$

$$b_{\pm k} = \frac{1}{2RT} \sum_{m=1}^{RT} F_s \left(\frac{m}{R} \right) \cos \frac{2\pi km}{RT} \pm \frac{1}{2RT} \sum_{m=1}^{RT} F_c \left(\frac{m}{R} \right) \sin \frac{2\pi km}{RT}$$

Having computed the 2WT pairs of coefficients, a_k and b_k , the 2WT coefficient C_k^2 are formed. Since only one signal is sought, it is the maximum of all the C_k^2 which need be compared to a threshold to make the detection decision. Since the threshold setting should be proportional to the noise power, β is chosen to achieve a given false alarm rate, or a given detection probability for a given signal-to-noise ration.

Table 2-2. Doppler Rates for the Forward and Return Links

RF Freq	Doppler Offset
User Satellite	
127.750 MHz	± 3.6 kHz
149	± 4.2
401	± 11.5
Ground Station	
137 MHz	± 7.6 kHz

The doppler processor has been implemented to cover the doppler uncertainty shown in table 2-2.

Actually the doppler processor has two modes of operation. Although it will operate with all the data rates specified in the forward and returns links, it will demonstrate optimal detection threshold for a 100 and 1000 BPS data rate link as summarized in table 2-3.

Table 2-3. Multimode Transponder Doppler Coverage:

Data Rate	Threshold (C/No)	Doppler Coverage
100 BPS	30 dB	± 4 KHz
1000 BPS	40 dB	± 16 KHz

2.4.7 COHERENT TRANSPONDER TECHNIQUE

Range and range rate between TDRS and user satellite are derived by use of a coherent transponder. The mechanization of the user satellite transponder is such that no demodulation of the received interrogation is required for derivation of range or range rate thereby avoiding time uncertainties involved in the demodulation of the received signal and remodulation of the transmitted carrier.

Range is measured strictly as a function of two-way transit time. The PN codes of both links, upon PN code acquisition are positioned in time on an a priori basis. The same code generator clock is employed for the return link transmissions and, upon attaining code synchronization, has its code position shifted in time to compensate for the range of the forward link.

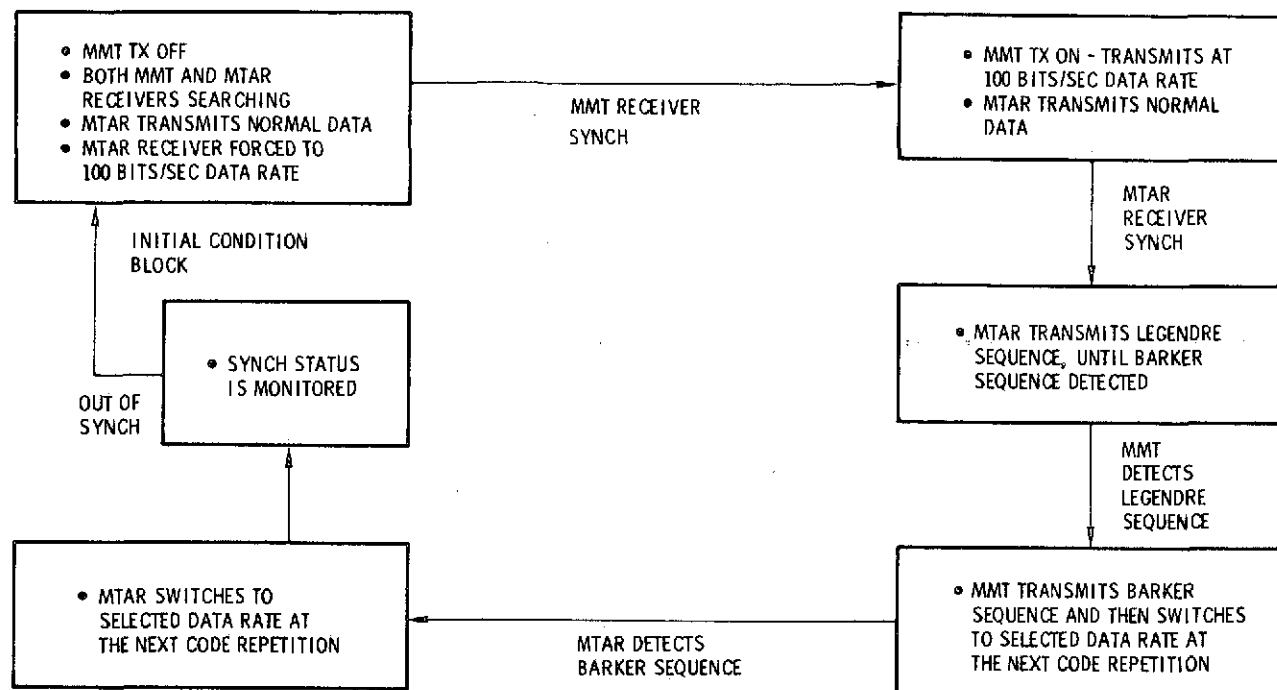
It is thus possible to measure the two-way range by simple comparison of the relative time position of the transmit encoder and the receive decoder. This is accomplished by measurement of the delay between its transmission and reception. The bandwidth extension resulting from PN modulation enhances the accuracy of measurement.

Range rate is derived from doppler effects on the carrier frequencies of both links. The links utilize separate carrier frequencies but, due to the technique for generating the return link carrier frequency, the forward and return link dopplers are additive.

The technique employed for synthesis of the return carrier is to merely translate the forward carrier to the desired return frequency. Thus, the forward link doppler is impressed on the return link transmission which is then further shifted at the MTAR receiver by the return doppler. The carrier frequency is thus shifted by the sum or difference of twice the doppler.

2.4.8 LINK ESTABLISHMENT IN THE PN MODE

Figure 2-20 shows the sequence of operations performed in both the MMT and MTAR to establish a duplex communications link. The box in the upper left hand corner is the state that the system will be in when the satellite is out of sight of the relay satellite. Whenever the earth blocks the transmission path between the TDRS



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Figure 2-20. Link Establishment Sequence

and the user satellite, both receivers will be out of sync and searching. Since the MMT transmitter (in transponder PN mode) will not be turned on until the MMT receiver is in sync, the sequence of acquiring sync will always be the same.

First, the MMT receiver searches until it synchronizes with the MTAR transmission. Once the MMT verifies the presence of a real synchronization point and not a multipath reflection, the MMT transmitter is turned and transmits at a data rate of 100 bits per second and a coder chip rate of 34.1166... kHz. The MTAR receiver which has been continuously searching eventually achieves correlation with the MMT transmission and verifies that it is not locking on a multipath transmission. After this verification from the MTAR, it interrupts the normal data stream to send a special sequence to the MMT. The one chosen is a 31 bit Legendre sequence. This sequence simulates the user address and command data that would be sent in a complete TDRS system with many simultaneous users.

Detection of this sequence at the MMT tells the MMT controller that the MTAR is in sync with the MMT's special transmission. The MMT controller now sends a 7 bit Barker sequence back to the MTAR to specify the time to switch from a

special acquisition transmission to a regular transmission. This process may seem rather complicated but it is required to provide (1) phase coherent data clocks for different data rates at each link and (2) reasonable acquisition in the return link which uses a long code to provide multipath rejection and a 1 megachip rate. The conflicting requirements of a long code repetition period to maximize multipath rejection versus a short code length to minimize search time become serious at the highest chip rate. The reason is that the number of chips in a 40 ms code repetition time is directly proportional to the chip rate while the time to search for correlation through a code depends solely upon the length of the code and not upon the chip rate of that code. The 30 to 1 factor in chip rates would mean a 30 fold increase in search time for the return link if the process described above were not used.

After all of the information transfer described above is completed both the MMT and MTAR receiver should be in sync and receiving data from the other end of the link. As long as they stay in synch no further steps are taken. If they drop out of sync a short search will be made to try to reacquire quickly. If that doesn't work the system will revert to the original state in the upper left hand corner of the diagram.

2.4.9 RANGE MEASUREMENT

In concept, two way range measurement is accomplished by computing the time differential between the transmitted PN code and the received PN code of the MTAR equipment. This concept was implemented by providing a "start pulse" from the "all ones" vector of the transmit code and a "stop pulse" from the "all ones" vector of the received code to a Time Interval Counter (commercial equipment) which calculates the delay interval in nanoseconds. The delay interval represents the two-way signal propagation time plus a constant delay due to the finite bandwidth of the receiver and transmitter ($2R + \text{Const.}$). Although the answer is in nanoseconds, it can readily be converted to feet or meters after subtracting the delay constant. Also, the answer is only valid after a PN transponding mode has been established as described in section 2.4.8 and is only available at "all ones" vector times (40 or 120 ms intervals, depending on the PN chip rate selection).

2.4.9.1 RMS Range Error

The expression for the RMS range error due to noise is expressed as, (on a worst case basis):

$$\Delta R_{\text{rms}} = \frac{c}{5} \sqrt{\frac{T_c}{2(S/N)_L}}$$

where

c = velocity of light

T_c = PN chip duration

$$(S/N)_L = \text{code loop SNR} = \left[\frac{C}{N_o} \left(\frac{1}{B_L} \right) \right]$$

C/N_o = carrier to noise ratio per Hz

B_L = the one sided code loop beamwidth

The carrier-to-noise density for the forward and return links, respectively, can be inserted into the above equation to determine the forward and return link rms range error. Estimate of range error includes all potential loss, RFI, multipath, other user signals and expected ambient Gaussian noise at the receiver.

2.4.10 RANGE RATE MEASUREMENT

In concept, two way doppler measurement is accomplished by computing the frequency error of the received signal with respect to the transmitted signal at the MTAR equipment in a transpond mode of operation. Two-way doppler measurement is possible in the application because the MMT equipment coherently translates its received signal to the selected transmit frequency, thus superimposing the doppler error of the forward link on to the return link.

Doppler error is measured by counting a 60 MHz LO generated from the 10 MHz VCO in the Costas loop of the MTAR receiver for an interval of time (1 or 10 seconds). A Frequency Counter (commercial equipment) is used to count the L.O. frequency using the 10 MHz reference oscillator of the MTAR transmitter as its "external frequency reference".

2.4.10.1 RMS Range Rate Error

The range-rate rms error in the forward and return links is determined from the standard range-rate error equation:

$$\Delta R_{\text{rms}} = \frac{C}{2\sqrt{2\pi}T_{\text{ob}} f_c \sqrt{(S/N)_L}}$$

where

C = velocity of light

T_{ob} = observation time

f_c = carrier frequency

$(S/N)_L$ = carrier tracking loop SNR $\left[= \left(\frac{C}{N_o} \right) \left(\frac{1}{B_{cL}} \right) \right]$

C/N_o = carrier-to-noise ratio

B_{cL} = carrier tracking loop Bandwidth

As in the aforementioned case, S/N ratios are inserted into equation to obtain an indication of the expected ΔR_{rms} for the forward or return links.

2.4.11 CONVOLUTIONAL ENCODER

Techniques are available and frequently employed, to detect and/or reduce error probabilities in decoding of digital communications. These techniques basically rely on the introduction of selected symbols at given points in a sequence of data bits. Those symbols and their positions are known at the receiver by virtue of a priori information. If, then, those particular symbols, as decoded, are in agreement with the pre-established sequence there exists some given relatively high probability that the data bits have also been correctly discriminated.

The methods of deriving types of positions and numbers of added bits has received significant mathematical attention. Ingenious techniques have been developed for attaining maximum error detection from inclusion of a given number of added bits. The addition of bits for error detection inevitably increases the baseband (where "baseband" is taken to include error detection bits as well as data bits) and the resulting reduction of S/N at the receiver requires high effectiveness of the error detection technique. In effect, a given investment of S/N reduction must be repaid by a high interest return on the error detection technique.

The convolutional encoder/decoder technique is highly efficient in error detection and, in addition, also permits error correction. It suffers only in the requirement for reasonably extensive computational facilities at the receiving terminal, a disadvantage which is essentially irrelevant in this instance since the receiving terminal is a ground base possessing extensive computing facilities.

Figure 2-21 shows a simple convolutional encoder of constraint length 3 and rate $1/2$.

For each data bit entered into the 3-bit register (its constraint length), two code bits are generated and transmitted. As is seen in the figure, the two code bits are a function of the entering data bit and the two previous data bits. There are eight combinations of new data bit and old data bits. These combinations and the pairs of transmitted code bits are shown in the state diagram, figure 2-22.

The column on the left shows the combinations of the two previous data bits (the one on the right is the oldest). The four combinations are represented by the "dots" at bit time T_{i-1} . The entering bit drives the register from the set of T_{i-1} states along the eight transition paths to the set of T_i states. The pairs of code bits generated by the register are shown just above each of the eight transition paths. For instance, if the previous data bits are 00 and the next bit is a 1, the register shifts from state 00 to state 10 and generates the code bits 11. This is shown by the path second from the top in figure 2-22.

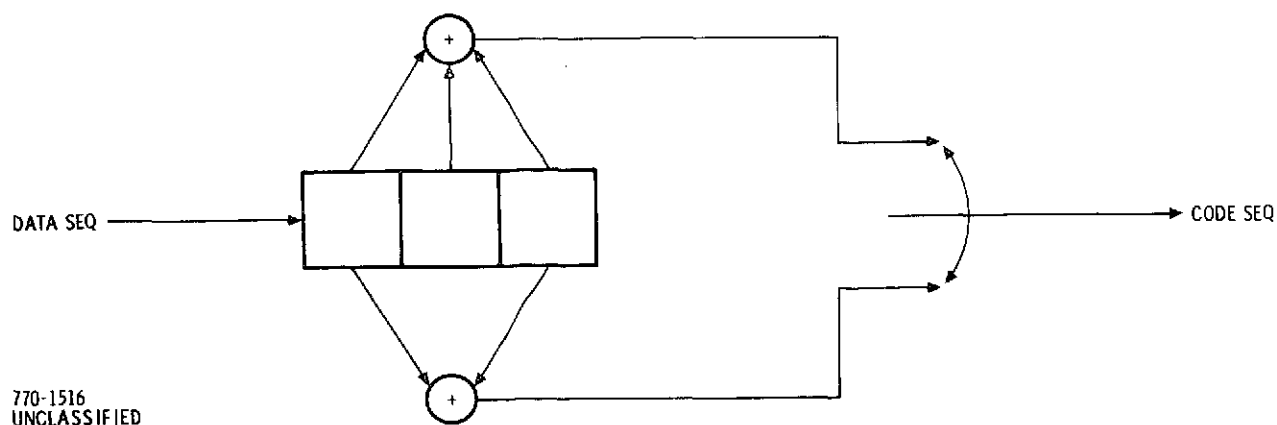


Figure 2-21. Conceptual Representation of the Convolutional Encoder

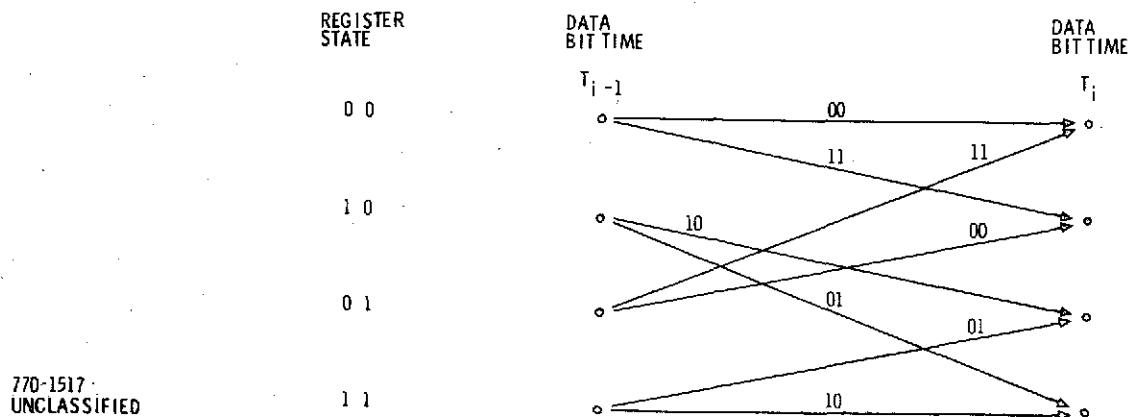


Figure 2-22. State Transition Diagram

An example is now introduced that illustrates the coding process. This example will be used later to illustrate the decoding process. The input data sequence is 00011100101. The input data and the resulting output code sequence is shown below.

Bit Time	T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}
Input Data Sequence	0	0	0	1	1	1	0	0	1	0	1
Output Data Sequence	00	00	00	11	01	10	01	11	11	10	00

By use of the state transition encoding diagram, it can be seen how the output code sequence is generated from the example data sequence. The encoder is in register state 00 initially.

The decoder works on the principle of Maximum Likelihood, i.e., it uses the optimal procedure that reproduces the data sequence most likely to have generated the received code sequence. It does this by constructing a state transition lattice and determining how well the received code sequence fits each of all the possible paths through the lattice. The path that has the closest match to the received sequence is the most likely path followed by the transmitting encoder. As shall be seen, an incorrect path accumulates a poor match with the incoming coded sequence and is terminated whenever it crosses a more probable path.

The decoder advances all of the probable paths one step for every pair of received code bits. As it steps, the probability of each path is updated by counting

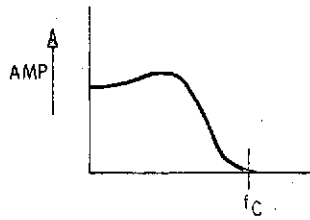
how many of the received code bits must be assumed wrong in order to take a particular path (0, 1, or 2). To illustrate the process, assume the decoder has received a pair of code bits 00. In the State Transition Diagram, Figure 2-22, the path passing through register state 00 may step to a new register state 00 without diminishing its probability because a 00 (received code bits) is required to make that transition. However, in order to step from RS 00 to RS 10 requires the assumption that both received code bits are in error since an 11 is required to make that step. Hence, the probability of that particular path is decreased by 2. The path passing through RS 10 branches to RS 01 and RS 11 with a probability decrease of one count for each. Also, RS 01 branches to RS 00 and RS 10 with probability losses of 2 and 0, respectively, and RS 11 branches to RS 01 and RS 11 with losses of one count each.

Which of the eight paths in the above example should be terminated due to having a low probability of being the correct path cannot be determined solely from the set of incremental losses in probability. This is determined by a running total of likelihood for each path. Whenever two paths meet at a common register state (e.g., RS 10 and RS 11 meet at RS 01), the decoder drops the least likely path from consideration.

2.4.12 VOICE CODING

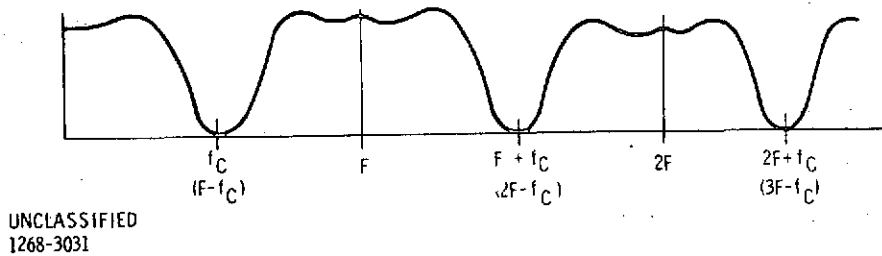
The multimode transponder uses PDM/PSK modulation for digitizing voice. This type of modulation permits near-optimum receivers that do not exhibit threshold in the range of operation of interest. The form of PDM is called SCPDM (Suppressed Clock PDM). As developed by MRL, SCPDM allows 100 percent modulation (negligible guard time) and transmits only information transitions by suppressing the clock transitions in the transmitter. These two features make SCPDM very efficient in terms of modulation theory. Since PDM is a form of pulse time modulation, it is required to sample the information in order to generate the basic pulse train.

Sampling techniques permit transformation of analog signals which are inherently two-dimensional variables, amplitude and time (frequency), into signals of one fixed dimension (sampling rate) and one variable (containing the amplitude information). The minimum sampling rate that permits perfect reconstruction of the analog signal (the Nyquist rate) is twice the highest frequency component of the analog signal. As an illustration, consider an analog spectrum extending to f_c as shown in figure 2-23. If this signal is sampled by multiplying it by unit impulses at a rate of $F = 2f_c$, the resultant spectrum is shown in figure 2-24. It is easily seen that if



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Figure 2-23. Analog Spectrum

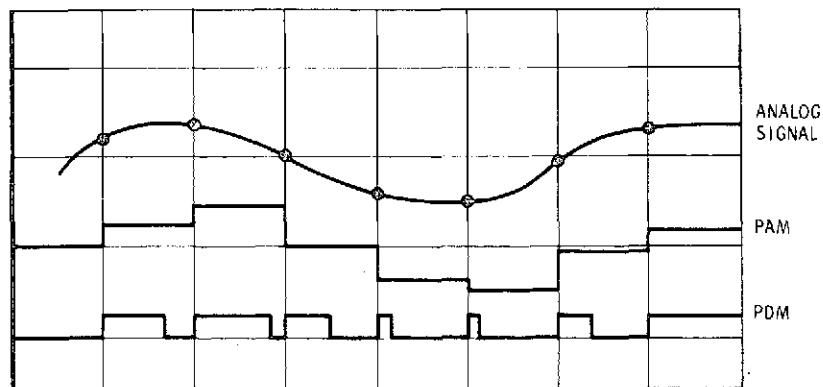


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Figure 2-24. Clocked Analog Spectrum

$f_c = F/2$, the upper and lower sidebands around $n \times F$ overlap producing an irresolvable ambiguity.

There are two basic modulation schemes associated with the sampled information: One varies a pulse amplitude to represent the sampled analog amplitude, and the other varies pulse timing to represent the analog amplitude. These are shown in figure 2-25.



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Figure 2-25. Two Types of Modulation for Sampled Information

The first scheme is called pulse amplitude modulation (PAM) and is the most rudimentary. The PAM receiver is a low pass filter. Since pulse amplitudes must be preserved in the RF receivers, PAM is identical to AM. It finds application in power-limited pulsed transmitters. The PAM samples are made narrow and large, and thus tower above the background noise during the "on" time. To realize the advantage, the receiver must be gated coherently.

The second scheme is called pulsed time modulation (PTM). One type of PTM is pulse duration modulation (PDM) or pulse width modulation (PWM). Here, the pulse width represents the analog amplitude. It is suited to constant-power transmission techniques such as PSK or FSK transmission. Signal recovery is optimized by an "integrate and dump" (I and D) filter following a hard limiter.

Any type of PTM requires a coherent clock. Pulse duration modulation usually uses the leading edge to transmit the clock and the trailing edge to transmit the analog information. An efficient way to receive PDM is to detect the crossovers. However, a more efficient way is to phase-lock a local oscillator to the leading (clock) edge of the samples and recover the samples by an I and D filter.

The technique developed by MRL goes one step further and has a very efficient transmission and recovery technique. The clock crossovers are deleted at the transmitter and are reinserted, essentially noiseless, at the receiver by means of a VCO loop. This halves the bandwidth of the principal sidebands of the transmitted signal, allowing a 3-dB improvement in the tracking of the Costas loop in the modem.

SECTION III

FUNCTIONAL DESCRIPTION

The Multimode Transponder and the Multimode Transmitter and Receiver Units are described in this section.

3.1 GENERAL DESCRIPTION

The section contains a description of the MTAR (ground) and the MMT (airborne) equipment developed for evaluating candidate modulation techniques for TDRSS.

The MTAR equipment consists of four chassis:

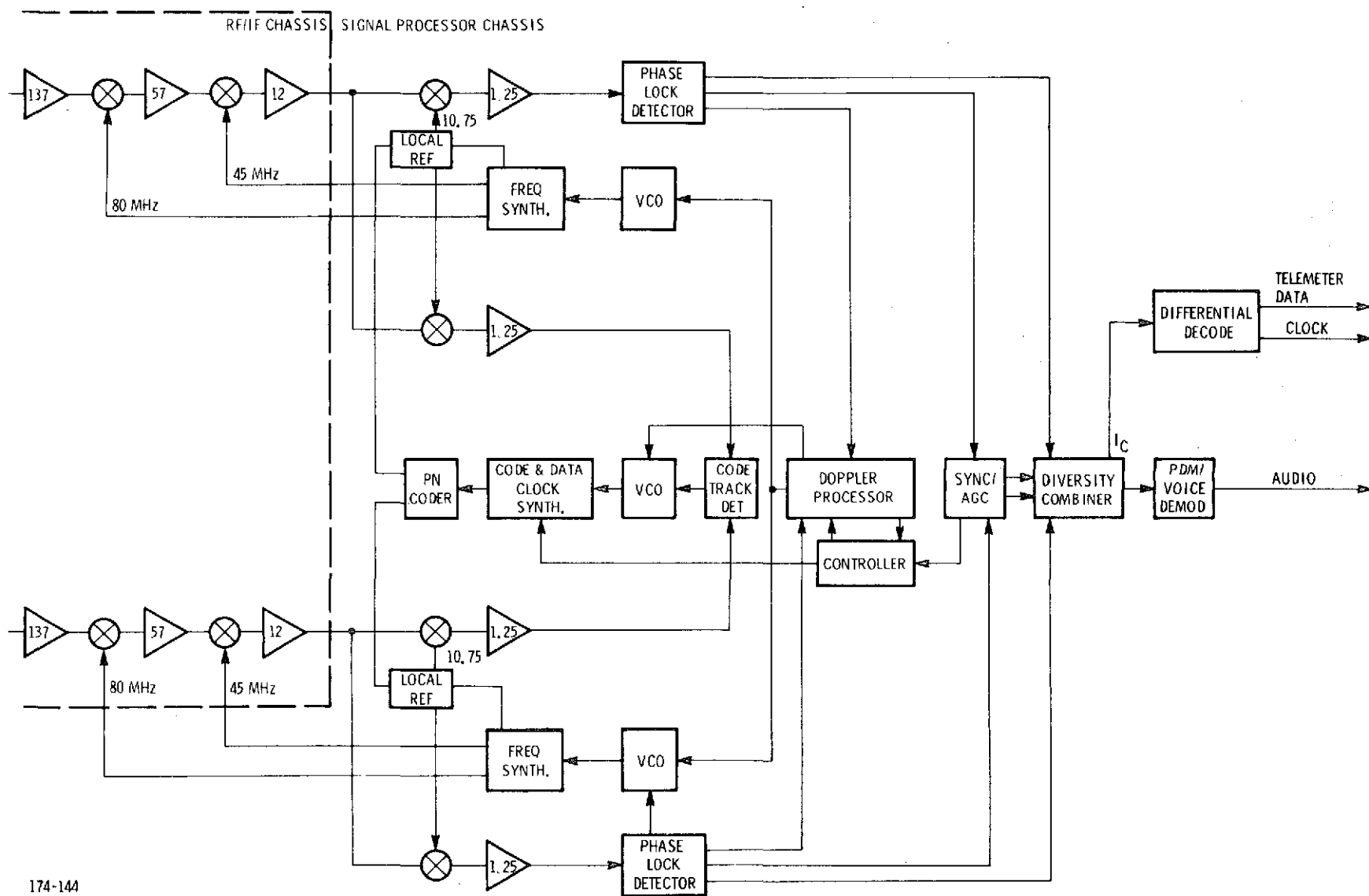
- a. The Receiver-Transmitter contains the RF to IF sections for both the receiver and the transmitter. It is shown in figure 3-1.
- b. The Signal Processor contains all circuits from IF to baseband for both the transmitter and receiver. It is shown in figure 3-1.
- c. The Power Supply provides all DC supply potentials to the other three chassis.
- d. The Control/Display Panel houses all mode selection switches and indicates the operational status of the equipment.

The MMT equipment also consists of four chassis which are similar in function and almost identical in appearance to the MTAR equipment.

3.1.1 MTAR EQUIPMENT

The MTAR consists of a diversity receiver and a transmitter operating through two quadriplexers into two antenna elements. The receiver functional block diagram is shown in figure 3-1. The first mixer converts the 137.0 MHz receive frequency down to 57.0 MHz. The IF amplifiers at 57.0 MHz and 12.0 MHz amplify the received signal.

The third mixer stage serves as a correlator in the pseudonoise mode of operation. The local reference circuitry balance modulates the receiver pseudonoise



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Figure 3-1. MTAR Receiver, Block Diagram

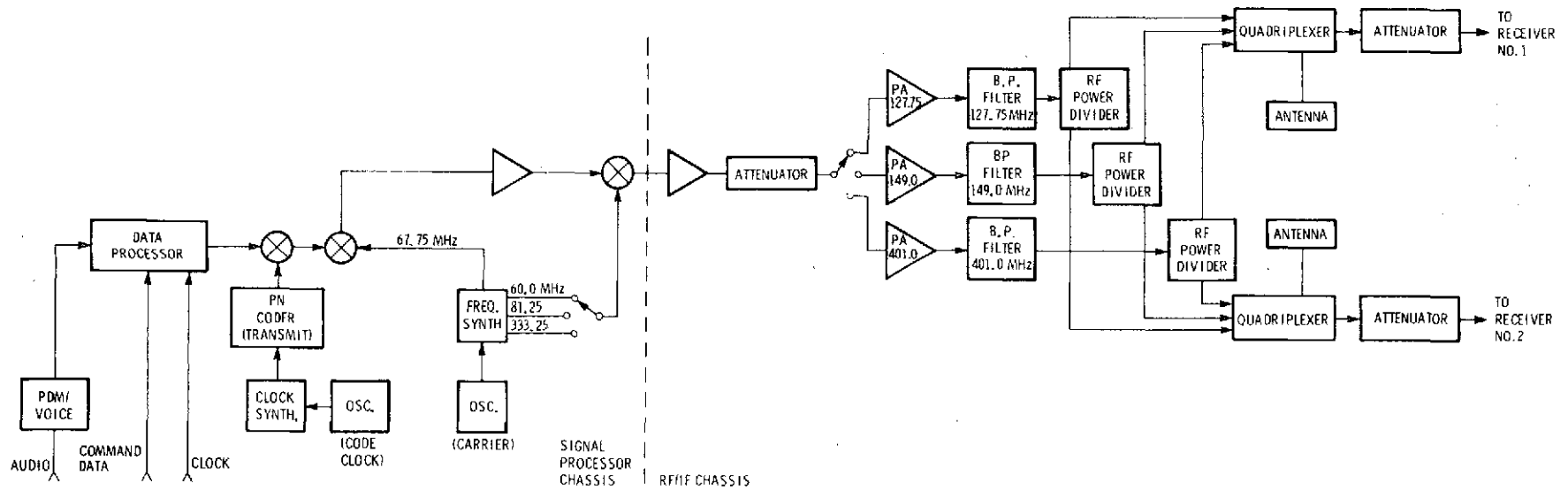
code with the 10.75 MHz local oscillator signal. When the code on the received signal is in phase with the locally generated code, a narrowband IF signal results. These signals are amplified and drive the phase-lock detectors in each of the two diversity receivers. When the incoming carrier signal is being tracked, each VCO provides a phase coherent drive to a frequency synthesizer which generates the receive local oscillator frequencies.

In the pseudonoise mode the code tracking loop keeps the receiver reference code in phase with the code on the received signal. In each receiver the incoming signal goes to a separate correlator and 1.25 MHz IF amplifier. The local reference provides this correlator with an early-late code from which a tracking error signal is derived. These error signals are combined and filtered in the code track detector and drive a single-clock VCO. Diversity reception requires two receivers because the propagation time difference due to the spatial relationship of the antennas is in the order of a full cycle at the RF carrier frequency. The code-track error signals can be combined to drive a single VCO because the 10 ns time difference in the received signals is insignificant at the code-chip rates used. The code and data-clock synthesizer is driven by the clock VCO and generates the selected chip-rate clock for the receive coder. In the conventional PSK mode the clock VCO and synthesizer are used to recover the received digital data clock.

The in-phase (I) outputs of the phase-lock detectors are combined in the diversity combiner. The telemetry digital data or PDM voice is extracted from the I-combined signal.

The doppler processor in conjunction with the controller searches out the doppler frequency uncertainty to obtain carrier lock. The anticipated doppler frequency error for the TDRS system is much greater than the carrier loop filter bandwidth. The doppler processor employs a technique that searches out the doppler uncertainty much faster than a linear cell-by-cell frequency search. Both the carrier frequency and code-phase uncertainties must be resolved. The controller advances or retards the code clock phase to obtain pseudonoise code synchronization. The sync-AGC circuitry makes the sync-search decision and generates the AGC signals to control IF amplifier gain.

The MTAR transmitter functions are shown in figure 3-2. The output amplifier drives into a variable attenuator for output power control. The attenuator is connected to the appropriate bandpass filter for the frequency to be transmitted.



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Figure 3-2. MTAR Transmitter, Block Diagram

An RF power divider for each of the bandpass filters provides the outputs to the dual quadriplexer and attenuator arrangement.

A frequency synthesizer driven by a stable crystal-controlled oscillator provides three transmit local-oscillator frequencies and the transmit carrier. One of the three local-oscillator frequencies is selected for mixing with the modulated 67.76 MHz transmit carrier to obtain the desired output frequency.

In the PSK mode digital data or PDM voice is balance modulated on the carrier. In the PN mode the digital data or PDM voice is combined with the pseudonoise code before being balance modulated with the carrier. The selected code-chip-rate clock is generated by a synthesizer driven by a stable oscillator at 10.24 MHz.

3.1.2 MMT EQUIPMENT

The MMT functions as a coherent transponder with the transmit carrier frequency synthesized from the receiver VCO tracking the forward link signal. The MTAR transmits to and detects the signal received from the MMT. Control box selection of modulation mode, command and telemetry data rates and pseudonoise chip rates, is provided. Digital data error rates can be measured both with and without convolutional encoding. A voice channel can be selected for both forward and return links. The return link carrier frequency will be 137.0 MHz while one of three frequencies (127.75 MHz, 149.0 MHz or 401.0 MHz) can be selected for the forward link.

The MMT consists of a diversity receiver and a transmitter operating through two quadriplexers into two antenna elements. The receiver functional block diagram is shown in figure 3-3. Selection of the expected receive frequency is made by selecting the appropriate input bandpass preselector and local oscillator frequency to the first mixer. Intermediate-frequency amplifiers at 67.75 MHz and 16.25 MHz amplify the received signal. The third mixer stage serves as a correlator in the pseudonoise mode of operation. The local reference circuitry balance modulates the receiver pseudonoise code with the 15 MHz local oscillator signal. When the code on the received signal is in phase with the locally generated code, a narrowband IF signal results. These signals are amplified and drive the phase-lock detectors in each of the two diversity receivers. When the incoming carrier signal is being tracked, each VCO provides a phase coherent drive to a frequency synthesizer which generates the local oscillator (LO) frequencies and transmit carrier frequency.

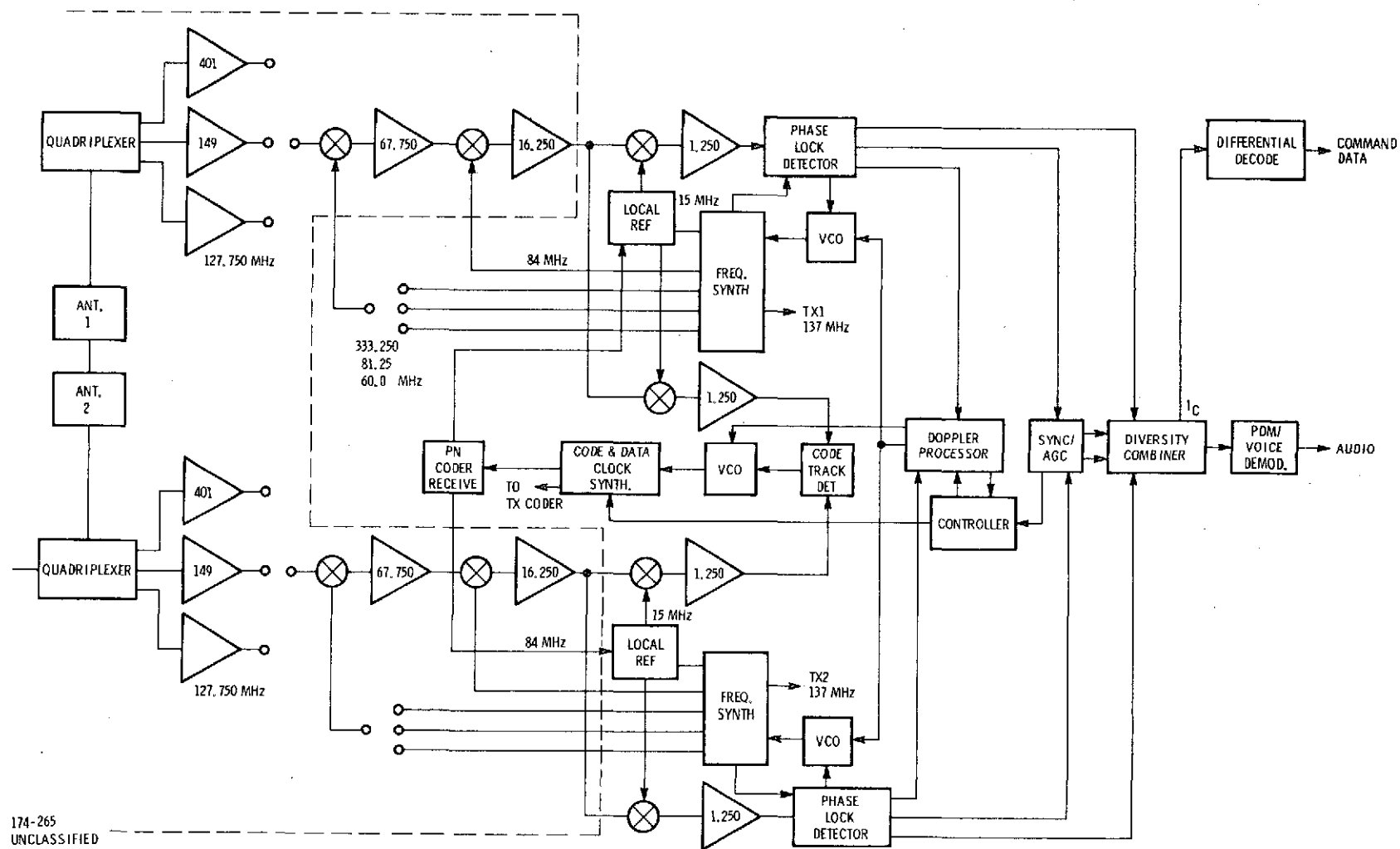


Figure 3-3. MMT Receiver, Block Diagram

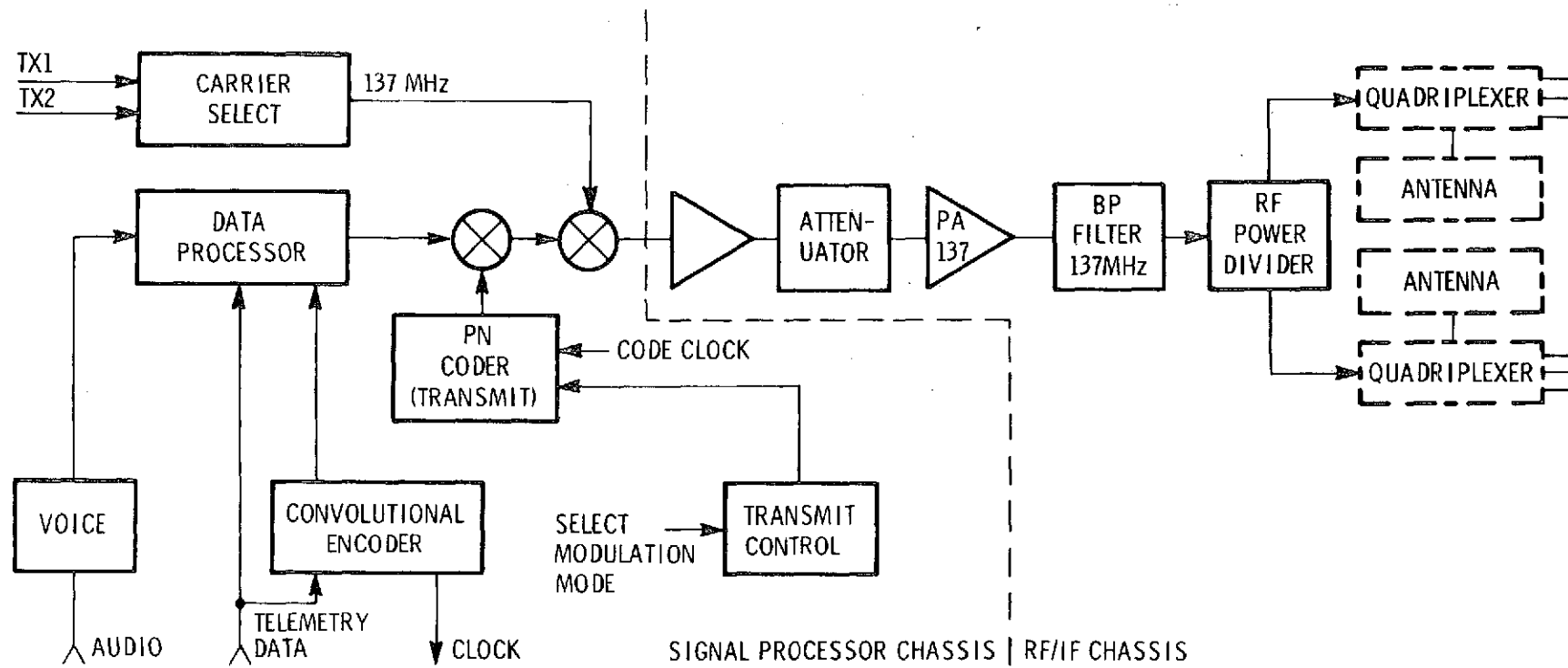
In the pseudonoise mode, the code tracking loop keeps the receiver reference code in phase with the code on the received signal. In each receiver the incoming signal goes to a separate correlator and 1.25 MHz IF amplifier. The local reference provides this correlator with an early late code from which a tracking error signal is derived. These error signals are combined and filtered in the code track detector and drive a single clock VCO. Note that diversity reception requires two receivers because the propagation time difference, due to the spatial relationship of the antennas, is in the order of a full cycle at the RF carrier frequency. The code track error signals can be combined to drive a single VCO because the 10 ns time difference in the received signals is insignificant at the code chip rates used. The code and data clock synthesizer is driven by the clock VCO and generates clocks for the receive and transmit coders. In the PSK mode, the clock VCO and synthesizer are used to recover the receive digital data clock.

The in-phase (I) outputs of the phase lock detectors are combined in the diversity combiner. The command digital data or PDM voice is extracted from the I-combined signal.

The Doppler processor, in conjunction with the controller, searches out the Doppler frequency uncertainty to obtain carrier lock. The anticipated Doppler frequency error for the TDRS system is much greater than the carrier loop filter bandwidth. The doppler processor employs a technique that searches out the doppler uncertainty much faster than a linear cell by cell frequency search. Both the carrier frequency and code phase uncertainties must be resolved. The controller advances or retards the code clock phase to obtain pseudonoise code synchronization. The sync/AGC circuitry makes the sync-search decision and generates the AGC signals to control IF amplifier gain.

The MMT transmitter functions are shown in figure 3-4. The output amplifier drives a power divider to provide outputs to the dual quadriplexer and antenna arrangement. Provision is made to adjust the output power level with a front panel control. The output amplifier is driven by a modulated 137 MHz RF signal. The carrier is selected to be taken from the frequency synthesizer of the diversity receiver phase locked to the strongest received signal.

In the conventional PSK mode the digital data or PDM voice balance modulates a carrier. In the PN mode the digital data/PDM is combined with the pseudonoise code before balance modulating a carrier. The transmit code clock is generated by the code and data clock synthesizer driven by the receive code clock VCO.



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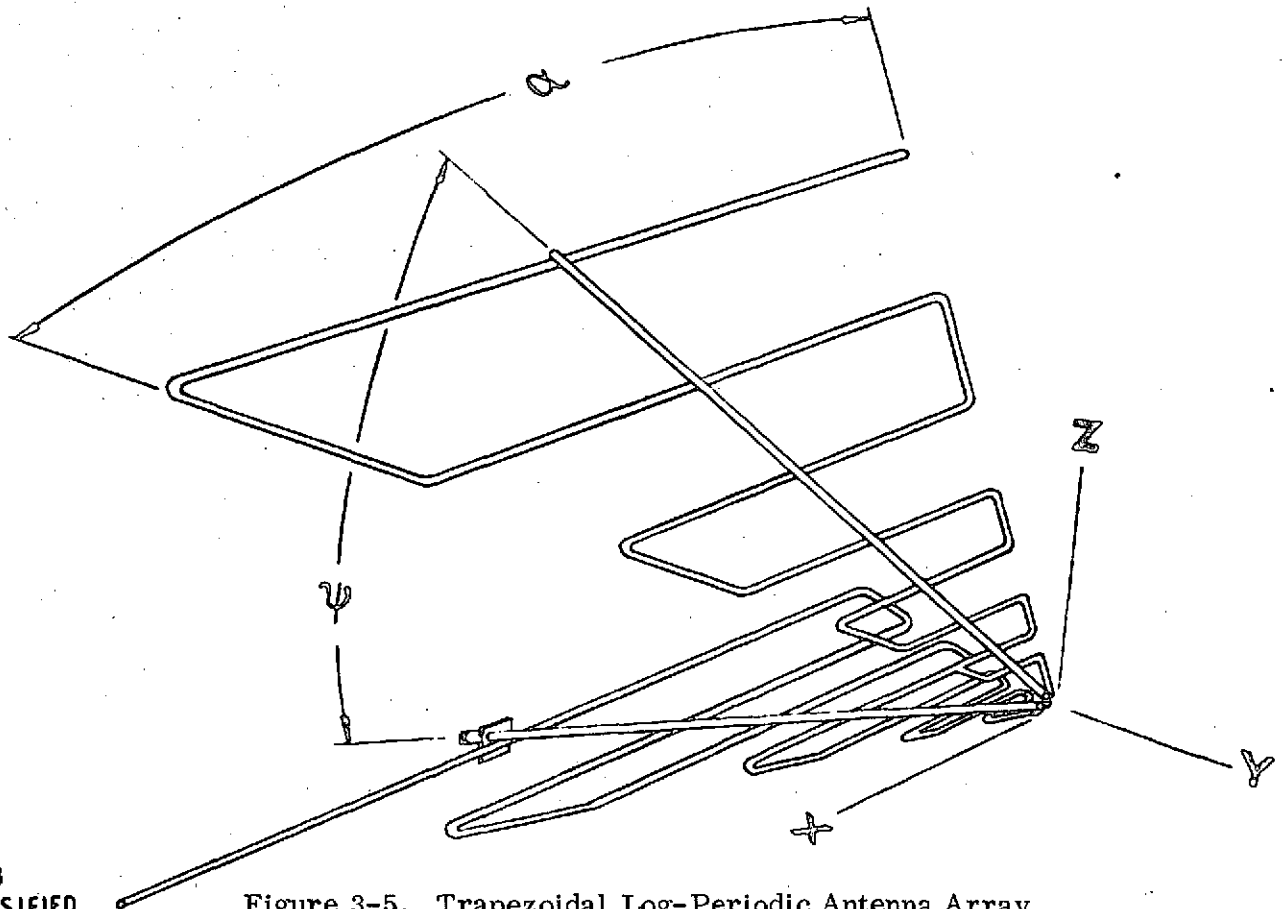
Figure 3-4. MMT Transmitter, Block Diagram

The telemetry digital data can be transmitted either with or without convolutional encoding. This feature allows for comparative data error rate tests to be run for evaluating performance improvement with convolutional encoding. A data clock output is provided to clock the external instrument that will generate the telemetry digital data.

3.1.3 MTAR ANTENNA

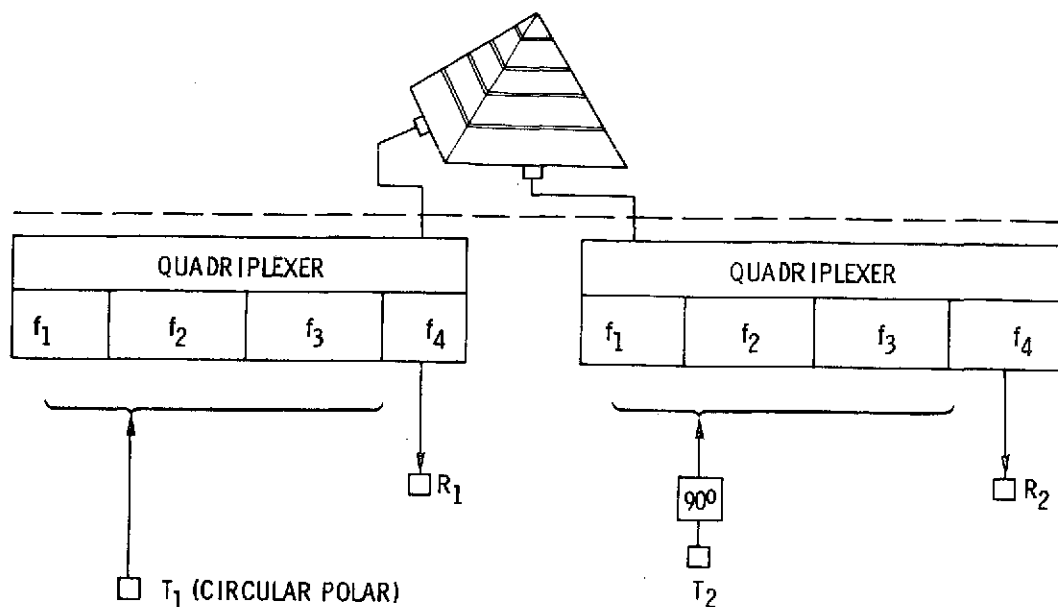
As part of the Multimode Transponder development program, an MTAR antenna was fabricated. This antenna was designed for use on the NASA van during flight testing.

The antenna is a coincident orthogonal trapezoidal log-periodic array. One of the two orthogonal arrays is shown in figure 3-5. The antenna consists of identical orthogonal arrays with dual coaxial outputs. These outputs are in-phase, but provide orthogonal linear polarization. They provide circular polarization when externally combined through an external 90-degree phase shifter as part of the terminal equipment. This antenna is used for simultaneous transmission and reception and requires a quadriplexer and phase shifter as shown in figure 3-6.



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Figure 3-5. Trapezoidal Log-Periodic Antenna Array



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Figure 3-6. Feed Schematic for Orthogonal Log-Periodic Arrays

Each array has the following electrical characteristics:

Frequency range:	126-402 MHz covering four discrete bands; 126-130, 136-138, 148-150, 400-402 MHz
VSWR:	2.0:1 maximum on 50 ohms in each frequency band
Outputs:	Dual 50 ohm coaxial
Pattern:	Unidirectional with each linear array displaying average half-power beamwidths of: E-plane = 65° H-plane = 70°
Front-to-Back ratio:	15 dB average
Gain:	6 dBm, each linear input

3.2 MMT (AIRBORNE UNIT)

The multimode transponder (MMT) consists of an RF/IF chassis, signal processor chassis, control box, and power supply chassis. This section gives a detailed functional description of each of these assemblies. Individual descriptions of each unique printed wiring board and subassembly are included. An antenna assembly for use with the MMT is specified but not supplied under this contract. The antenna specified is identical to the one supplied for the MTAR. The MTAR antenna assembly is described in section 3.4.

3.2.1 RF/IF CHASSIS

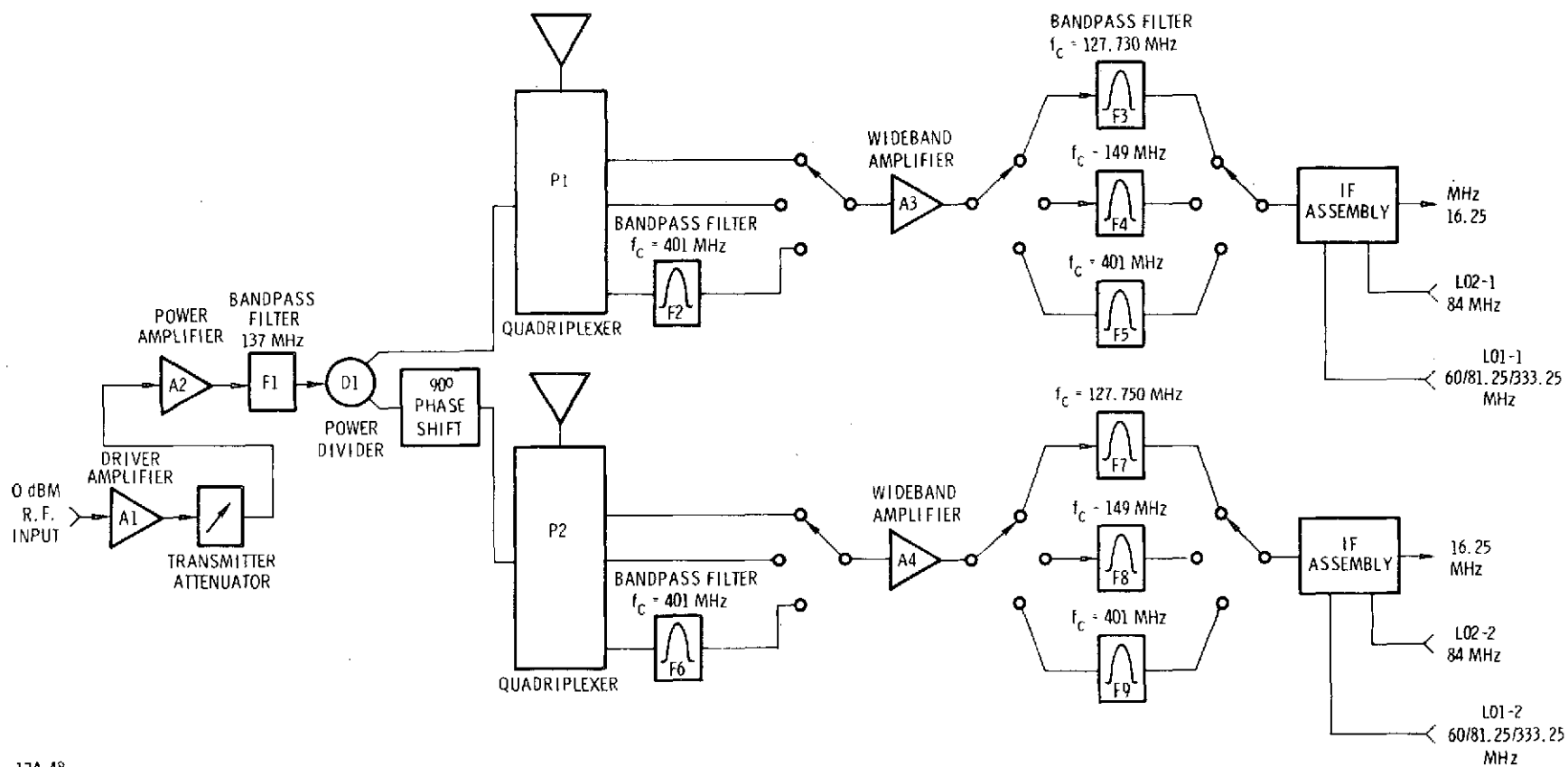
The RF/IF chassis contains the high frequency, high power modules that are cabled directly to the antenna connections. There is an antenna port for each of two quadriplexers which isolate transmit power from the receiver inputs. The RF output from the modulator is amplified to the chosen transmit power level in the RF/IF chassis. The RF/IF chassis contains front end amplification, bandpass filtering, and frequency conversion for each of the two diversity receiver channels. Each of the functional elements shown in figure 3-7 is described in the following paragraphs.

3.2.1.1 Driver Amplifier (A-1)

The driver amplifier module amplifies the RF signal from the modulator. This module uses a type CA 801 broadband RF amplifier. The driver module contains an input resistive network for impedance matching and gain setting. A voltage regulator drops the + 28VDC to the + 24 VDC required by the CA 801.

3.2.1.2 RF Power Amplifier (A2)

The RF power amplifier is a commercial, solid-state, amplifier. The amplifier is a unique combination of lumped elements, microstripline and ferrite hybrid techniques. The design insures stable performance and high reliability over the temperature range. The input drive will be supplied at a power level of 0 dBm and a frequency of 137 MHz. The total gain of the driver amplifier and power amplifier is approximately 36 dB and all intermodulation products and spurious responses are down at least 30 dB. The input drive will be a constant envelope carrier. The output power is adjustable in 1 dB steps over a 60 dB range. The power amplifier can deliver 4 watts into a 50 ohm load. The output stage is protected and will not be damaged as a result of the output port being indefinitely opened or short circuited. The DC power requirement for the power amplifier is + 13.8 VDC regulated from + 15 VDC and power efficiency is greater than 30 percent.



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Figure 3-7. MMT RF/IF

3.2.1.3 Transmitter Bandpass Filter (F1)

The power amplifier is followed by a bandpass filter (F1) which limits the output amplifier to a center frequency of 137 MHz and a 4-MHz, 3-dB bandwidth. The bandpass filter has an 18 MHz, 45 dB bandwidth, that is used in conjunction with the quadriplexer. The bandpass filter and the quadriplexer supply 110 dB of isolation between the transmitter band and the receiver bands. The bandpass filter insertion loss is less than 2.4 dB. The 137 MHz bandpass filter's characteristics are specified in drawing X625267-2.

3.2.1.4 Power Divider (D1)

The power divider is used to divide the output signals of transmitter bandpass filter (F1). The device is 3 dB hybrid coupler employing strip transmission line techniques. Power division difference at the outputs is in the order of 0.5 dB. The output signals are 90 degrees out of phase with each other. The bandwidth of the device is 125 MHz to 250 MHz.

3.2.1.5 Quadriplexers (P1 and P2)

The outputs of the power divider D1 are routed into the 137 MHz ports of the quadriplexers. A quadriplexer permits the use of a common antenna for transmission and reception. Each unit drives one antenna input at a VHF frequency of 137 MHz. The antenna receives and drives the quadriplexers with one of three frequencies, two VHF frequencies (127.750 MHz and 149 MHz) and one UHF frequency of 401 MHz. The two VHF and one UHF frequencies are routed to the corresponding preselector bandpass filters. Each quadriplexer has a total of five ports, which are (1) 137 MHz, (2) 127.750 MHz, (3) 149 MHz, (4) 401 MHz and (5) the antenna port. The quadriplexers must have adequate isolation since transmitter and receivers are on at the same time. To maintain separation of the transmitter frequency from the receiver frequency, a 110 dB isolation is required between the transmitter band and receiver band. Refer to table 3-1 for a summary of isolation necessary to obtain separation. The design for the required quadriplexers provides 70 dB of isolation between bands. The other 40 dB is obtained from the bandpass filters.

3.2.1.6 Preselector Bandpass Filters (F2-F9)

Quadriplexer (P1) supplies drive to bandpass filters centered at each of the three receive frequencies. The filters are used in conjunction with the quadriplexer

(P1) to obtain a 110 dB of isolation between the transmitter band and the receiver band. The bandpass filters are tuned to have the following characteristics: The F3 center frequency is 127.750 MHz and has a 3 dB bandwidth of 10 MHz, F4 center frequency is 149 MHz and has a 10 MHz 3 dB bandwidth, F2 and F5 center frequency is 401 MHz and has a 10 MHz 3 dB bandwidth. All receive filters have a 60 MHz, 40 dB bandwidth. Quadriplexer (P2) similarly supplies drive to three receive frequency bandpass filters F6 through F9.

Table 3-1. Transmitter-Receiver Isolation Requirements

$$\text{ISOLATION REQUIREMENTS} \geq (30 + 136 + 10 \cdot 20 \log \pi \frac{\Delta f}{f_c} - 10 \log \frac{f_c}{f_b}) \text{ dB}$$

WHERE: Δf = FREQUENCY SEPARATION
 f_c = CHIP RATE
 f_b = DATA RATE (100 BPS)

Δf (MHz)	f_c (KHz)	$20 \log \frac{\Delta f}{f_c}$ (dB)	$10 \log \frac{f_c}{100}$ (dB)	Transmitter Power in Receiver Bandwidth (dBm)	Isolation Necessary (dB)
137-127.750 = 9.250	1024	29	40	-39	107
	102.4	49	30	-49	97
	34.1	59	25	-54	92
149-137 = 12	1024	31	40	-41	105
	102.4	51	30	-51	95
	34.1	61	25	-56	90
401-137 = 264	1024	58	40	-68	78
	102.4	78	30	-78	68
	34.1	88	25	-83	63

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3.2.1.7 Wideband Amplifiers (A3 and A4)

The selected receive frequency signal is amplified by a wideband amplifier for each of the two diversity receiver channels. An Avantec UTA-395 wideband amplifier provides 30 dB of gain in each receive channel. For each selected receive frequency the input to each amplifier is connected to the appropriate quadriplexer port and the output is connected to the corresponding bandpass filter.

3.2.1.8 I.F. Assembly

An intermediate frequency assembly for each receiver amplifies and translates the received signal down to 16.25 MHz. The frequency translation is done in two steps with filtering and amplification at an IF frequency of 67.75 MHz. The input

to the IF assembly is connected to the appropriate bandpass filter for each of the selected receive frequencies. The local oscillator signals are generated and selected in the Signal Processor Chassis and brought to the RF/IF chassis via coax cables. In addition to frequency translation and amplification, the IF assembly includes non-coherent AGC circuitry to maintain a maximum 16.25 MHz IF signal level of -24 dBm. The schematic of the IF assembly is drawing X498729.

3.2.2 SIGNAL PROCESSOR CHASSIS

The MMT signal processor chassis contains the receiver circuitry from the 16.25 MHz If down to baseband processing and the transmitter modulation circuitry. The MMT signal processor chassis is made up of plug-in printed-in boards. The following is a list of board nomenclature and the quantities used in the MMT:

Assembly Dwg. No.	Printed Circuit Board Nomenclature	Quantity	MMT Location	
X918051	Code and Data Clock Synth.	1	2A08	
X918052	Coder	1	2A07	
X918054	Controller No. 1	1	3A03	
X918047	Controller No. 2	1	3A02	
X918057	MMT Local Ref/Correlator	2	1A09	3A09
X918058	Baseband Conditioner	2	1A08	3A08
X918059	Carrier Track	2	1A07	3A07
X918060	Code Track	1	2A09	
X918066	PDM Voice	1	2A02	
X918070	TX Data Processor	1	1A02	
X918063	Data Recovery	1	1A03	
X918064	Doppler Input	1	3A04	
X918065	Doppler Arithmetic	1	2A04	
X918090	Doppler Control	1	2A05	
X918092	Doppler Output	1	1A04	
X918067	MMT/MTAR Synth No. 1	2	1A06	3A06
X918068	MMT Synth. No. 2	2	1A05	3A05
X918071	MMT/MTAR Modulator	1	2A03	
X918093	RF Switch	1	2A06	

A functional description of each type of printed-circuit board used in the MMT follows.

3.2.2.1 Local Reference/Correlator Board

The local reference/correlator module (figure 3-8) contains: (1) the AGC portion of the 2nd IF of the receiver's triple-conversion RF-IF circuitries, (2) correlators and 3rd IF for the carrier and code-tracking loops, and (3) logic to generate the bogey and early-late reference signals used in the correlator for PN mode operation.

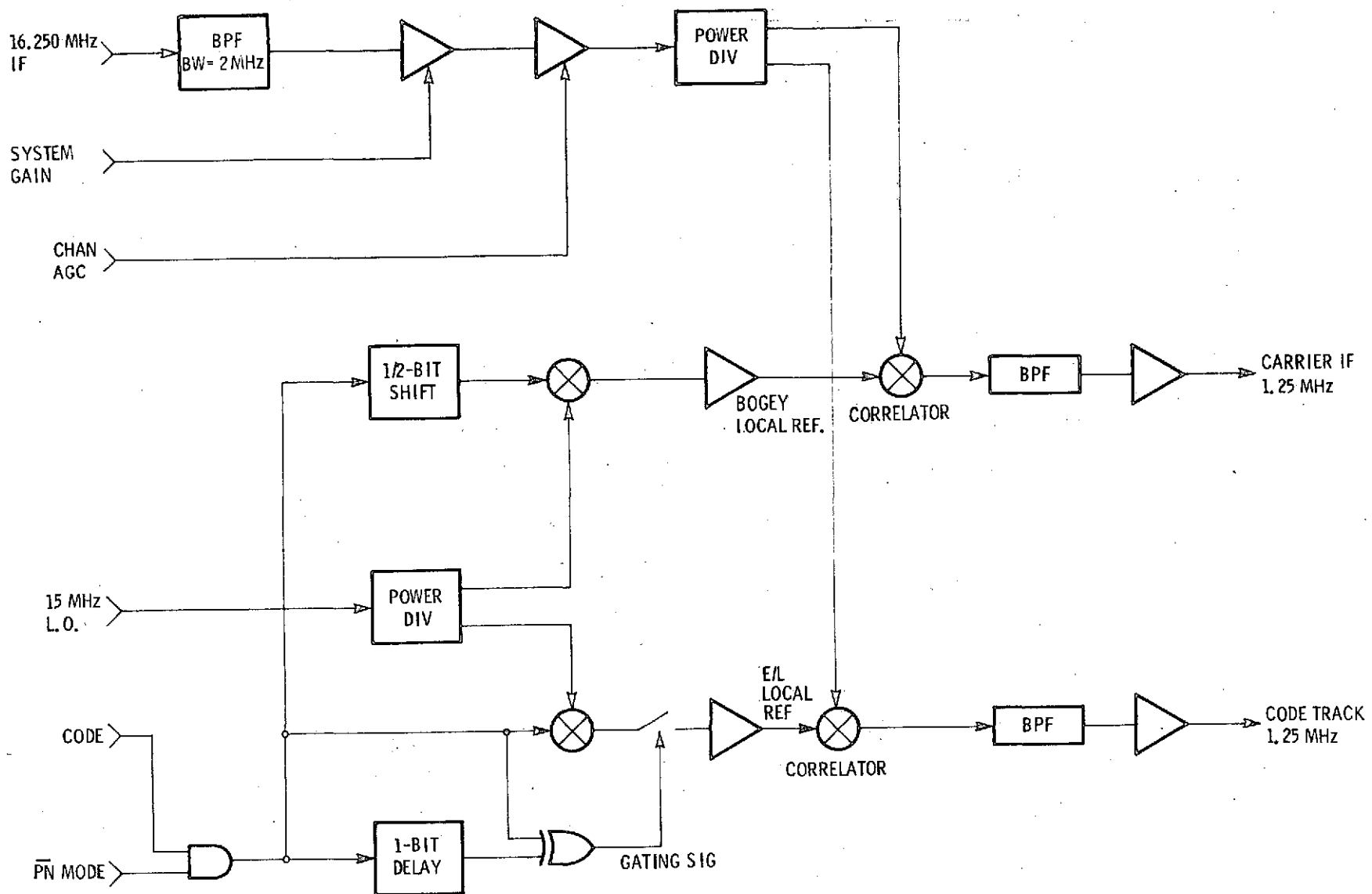
The AGC function in the 2nd IF is carried out by two control signals: namely, System Gain AGC and channel AGC. System AGC provides a fixed setting for RF gain to optimize the channel AGC range. Channel AGC is derived from estimates of each receiver's own received signal power.

In the PN mode, the spread-spectrum signal from the second IF is correlated with two local reference signals to generate two separate IFs, one for carrier tracking and the other for code tracking. Except for the local reference signals used in the correlation process, the two correlator-mixers and the third IF's characteristics are identical. They are both band limited to 125 kHz and have 40 dB gain.

The correlation process in the carrier and code correlators is best illustrated in figure 3-9.

In the carrier correlator, the incoming code, waveform A, is correlated with the local-bogey code, waveform E. If the relative displacement between waveforms A and E is τ , the carrier correlator output will be as shown in waveform F, which when averaged yields value less than 1. At code sync, τ is zero and the carrier correlator output will be a steady 1, a maximum correlation condition.

In the code-loop correlator, the incoming code is correlated with the local late code, waveform B. But the correlation is gated on and off by waveform C, which is the resulting code of modulo-two addition of the late code PN ($-\tau/2$) and an early code PN ($\tau/2$) (early and late codes are $\pm 1/2$ chip with respect to the bogey code). Thus, if there exists a code displacement τ , the code-loop correlator output will be as shown in waveform D, which when averaged yields a positive error signal. As τ is varied, the so-called S-error curve, depicted in figure 3-10 is generated. The figure shows the desired error signal for code tracking.



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Figure 3-8. Block Diagram-Local Reference/Correlator

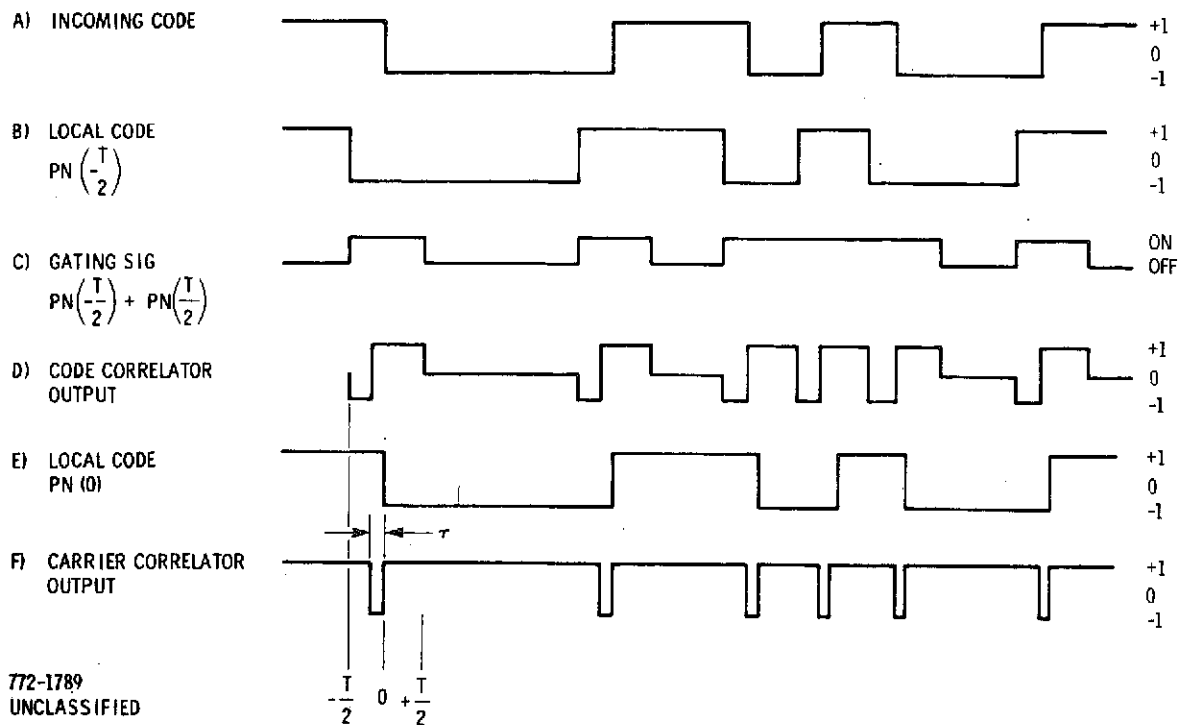
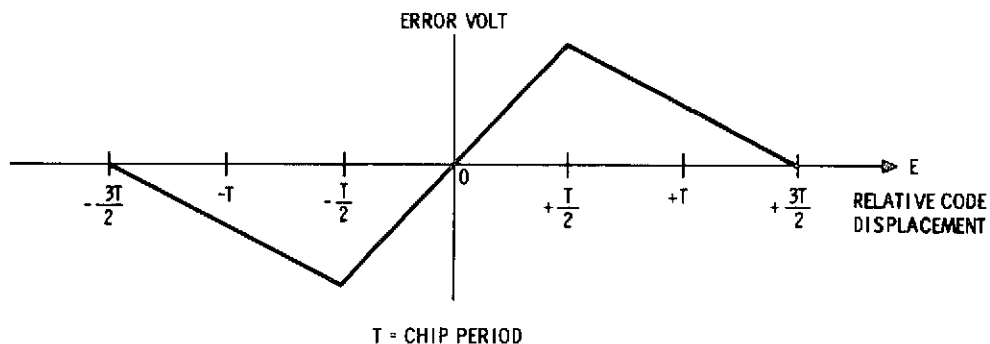


Figure 3-9. Correlation Process Waveforms



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Figure 3-10. S-Error Curve

In the conventional mode, incoming carrier is not modulated by PN code. Thus, to operate the receiver, the local code is inhibited so that the carrier correlator functions only as a regular mixer. The code-correlator IF is not used.

3.2.2.2 Baseband Conditioner Board

The baseband conditioner (figure 3-11) consists of the final receiver mixing operation and low-pass filters, which reduce incoming signals to baseband or "zero"

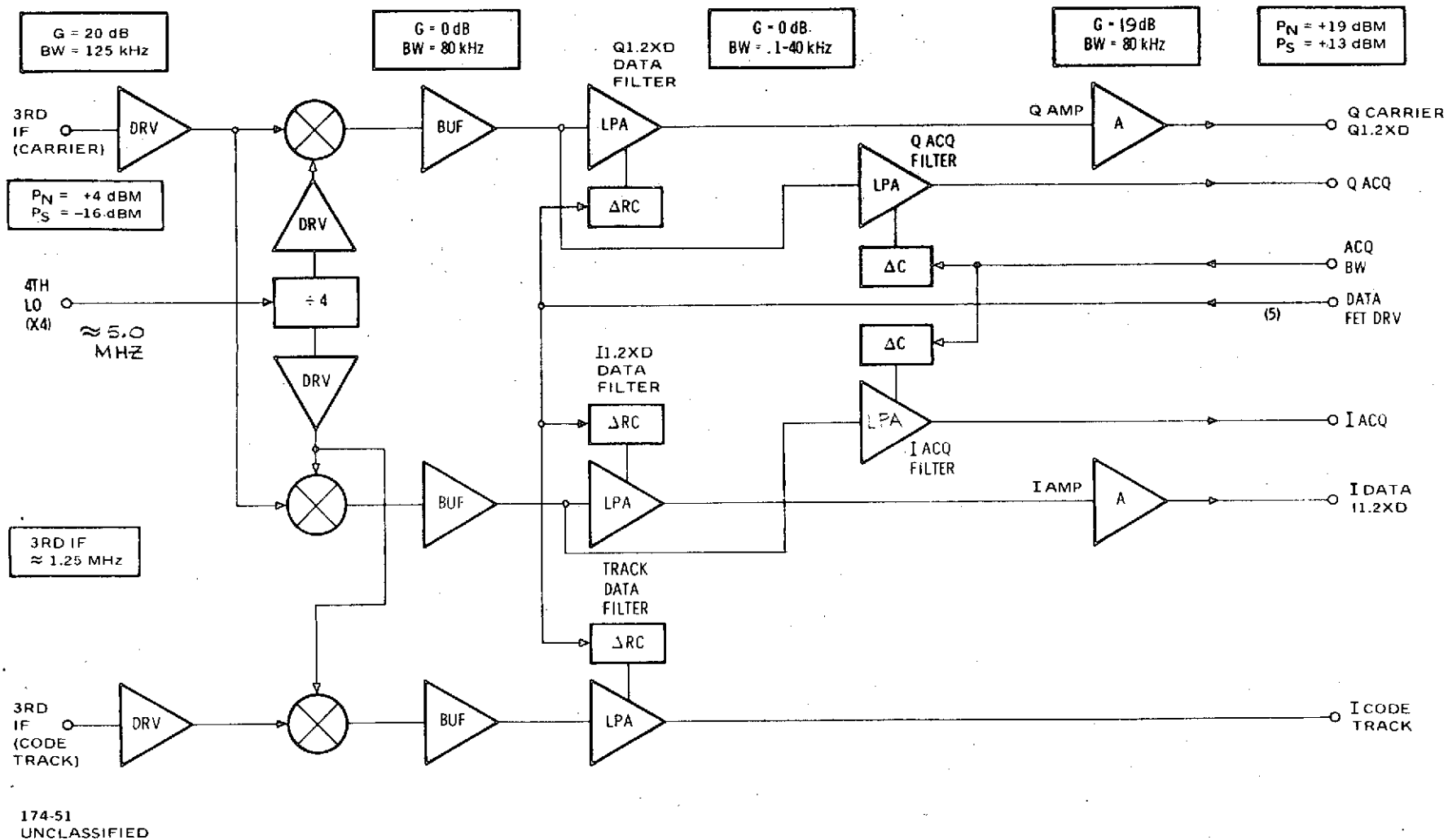


Figure 3-11. Baseband Conditioner - Block Diagram

IF. The block diagram shows two separate third IF inputs and a fourth local oscillator, operating at four times the third IF or ≈ 5 MHz. The data (carrier) third IF drives two high-level I and Q demodulators, supplied with references of quadrature phase, developed by different stages of the divide-by-four.

The code track third IF input is obtained from a separate track receiver channel, and contains PN code-tracking error information. This drives a third high-level demodulator using the same in-phase or I reference as the I data demodulator. Since the fourth local oscillator and third IF are at the same nominal frequency, the output of all three high-level demodulators will be the effective Doppler rate between the incoming signal and the internal precision reference.

A marginal, near-threshold signal will have a signal power of ≈ -16 dBm at the third IF inputs, while noise power will be $\approx +4$ dBm, measured in the 125 kHz third IF bandwidth. A gain of 10 dB is provided by the drivers, while the demodulators themselves convert the signals to baseband with very little loss (< 0.5 dB). After filtering the now baseband signals are buffered by a unity gain noninverting amplifier, and bandwidth limited to 80 kHz. Total noise power will be $\approx +12$ dBm while the signal power is ≈ -6 dBm.

All three baseband demodulator filter outputs e.g., I DATA, Q CARRIER, and CODE TRACK, are now bandwidth limited by their respective data filters at 1.2 times the effective data rate. A closed-loop feedback type of single-pole active filter provides 6 dB per octave rolloff at corner frequencies that are 1.2 times higher than the incoming data rates. This assumes minimum interbit distortion and noncritical component selection. An arrangement of FET switches select resistor and capacitor combinations as well as open-loop amplifier gain setting resistors to vary the corner frequency for each discrete data rate situation.

These 1.2XD data filters present a restrictive aperture to the total baseband noise power, and the signal-to-noise ratio is considerably enhanced. If marginal signal power is assumed to produce a signal-to-noise ratio of +10 dB in a matched data filter (BW = data rate), then the signal-to-noise ratio at threshold will be +7.8 dB at the output of the 1.2XD filters.

The 1.2XD filter outputs drive their respective 19 dB gain amplifiers. The Q amplifier output is sent to the individual receiver carrier track loop, while the I amplifier output goes to the I combiner to extract data. Tracking channel amplifier output is sent to the track combiner to effect common code track.

Inputs of the I and Q 1.2XD data filters also go to the I and Q acquisition filters respectively. The bandwidth of these filters is set at 4 kHz or 12 kHz, depending on the Doppler acquisition mode selected. Two poles provide 12 dB per octave rolloff and +19 dB in-band gain. The noise power in the 4 kHz acquisition bandwidth is +19 dBm while the threshold signal power is +13 dBm, assuring the -6 dB minimum signal-to-noise ratio required for the 100 Hz BW Doppler processor scheme.

NOTE

$$4 \text{ kHz to } 400 \text{ Hz} = 10 \text{ dB}$$

$$\begin{array}{l} 400 \text{ Hz to } 100 \text{ Hz} = \frac{6 \text{ dB}}{16 \text{ dB}} \\ \text{S/N improvement} \end{array}$$

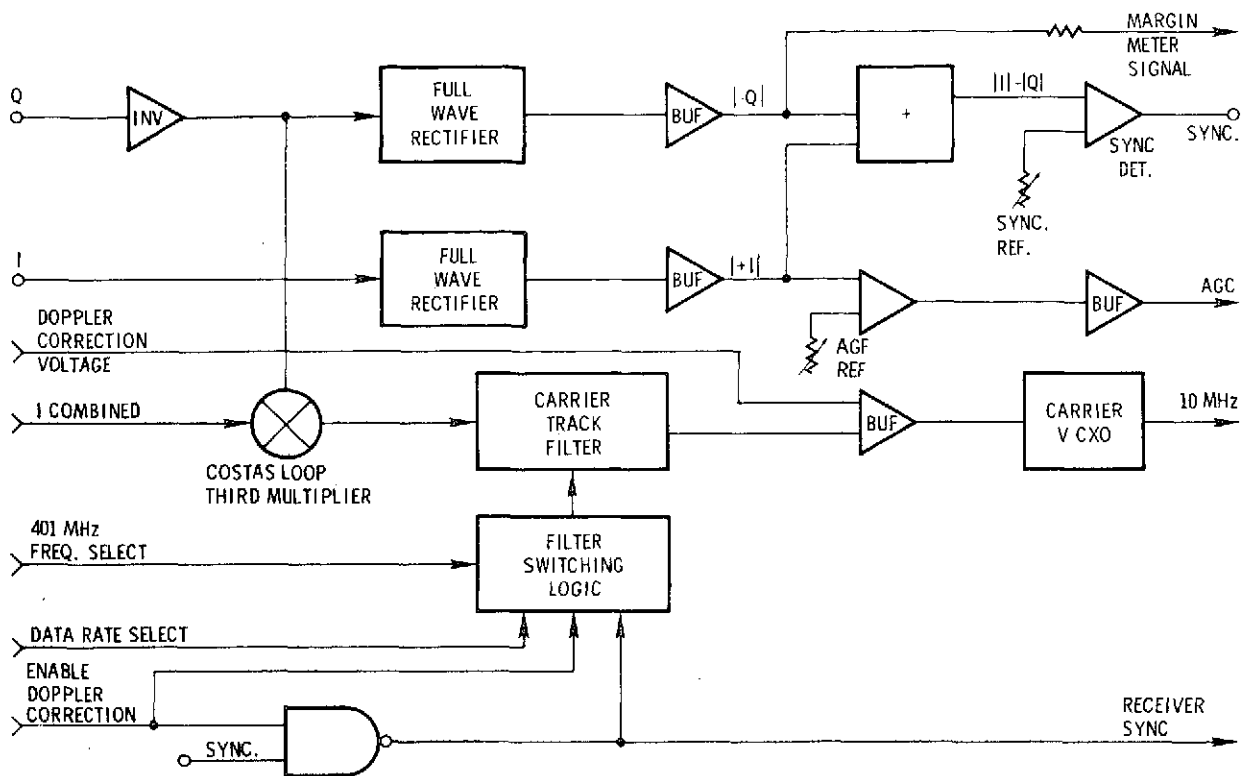
$$\text{S/N @ } 100 \text{ Hz} = \text{S/N @ } 4 \text{ kHz} + 16 \text{ dB} = +10 \text{ dB}$$

3.2.2.3 Carrier Track Board

The carrier track board essentially completes the loop of the phase lock detector. Circuitry for the carrier phase lock detector is contained on a Baseband Conditioner Board and a Carrier Track Board for each of the two diversity receivers. The Carrier Track Board gets the I and Q signals that were quadrature detected and filtered on the Baseband Conditioner Board. Receiver sync and AGC signals as well as the control signal for the carrier VCO are derived from the I and Q analog inputs.

The carrier track board contains the carrier loop third multiplier, filter and voltage-controlled crystal oscillator which supplies the input reference for the frequency synthesizer. As shown in the functional block diagram (figure 3-12) the I and Q inputs are full wave rectified to obtain absolute values from which a sync decision and channel AGC signals are derived. The output of the third multiplier is filtered, summed with the doppler correction voltage and drives the control input of the carrier VCXO. The 10 mHz output of the VCXO drives the frequency synthesizer for the appropriate receiver. The enable doppler correction is a digital signal from the controller that is anded with the sync decision from the phase locked loop detector.

The carrier loop filter is changed for different modes of operation by FET switches controlled by mode selection logic. The loop filter time constant is changed for the data rate selected. The loop gain is changed for the receive frequency selected. The receiver sync signal determines the search or track loop bandwidth.



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Figure 3-12. Carrier Track Board

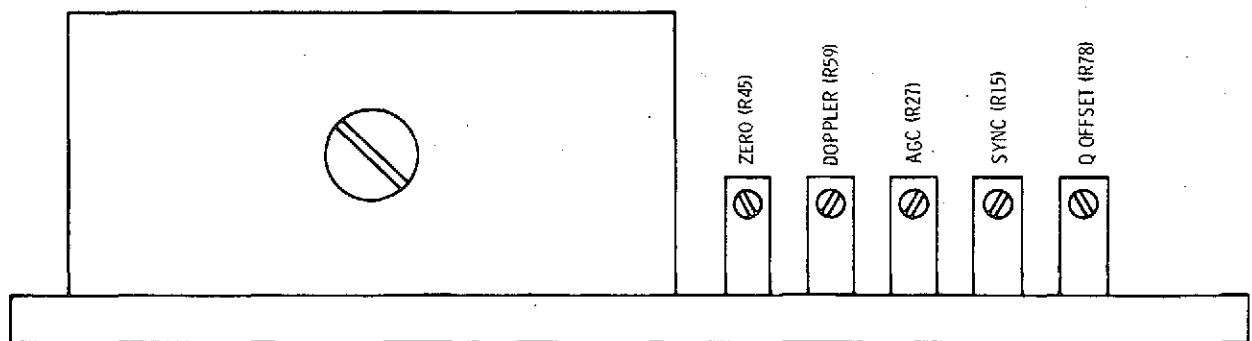
The enable doppler correction signal causes the loop filter output to be dumped to zero volts while the doppler processor is determining the receive frequency uncertainty. During this time the analog doppler correction voltage is controlling the carrier VCXO frequency. When the doppler processor in conjunction with the controller determine the doppler frequency offset, the doppler correction voltage remains fixed and the carrier loop filter is no longer held to a zero volt output. The Costas loop can then acquire and track the received signal.

The carrier loop's tracking bandwidth is set at 20 Hz, which is high enough to provide adequate response for the acceleration of low-altitude satellites, while minimizing the tracking noise perturbations associated with greater loop bandwidths. During acquisition, the loop bandwidth is increased to 80 Hz, to provide greater pull-in range and response. The large tracking loop capacitor is forced to assume the offset of the smaller acquisition filter, so that it can be inserted in the loop at sync without introducing a large velocity error. This forcing and switch-over is effected by two FET switches or gates.

To keep the tracking loop bandwidth constant at 20 Hz, the open loop gain must be decreased when operating in the 401 MHz band to compensate for the increased VCO multiplier or ΔXN term. This ΔXN is proportional to the ratio of the high band 401 MHz to the average low band of ≈ 138 MHz. Open loop gain must therefore be reduced by $\frac{138}{401} = 0.32 \approx -5$ dB, effected by changing the VCO buffer amplifier summing resistor with an FET driven by the 401 band select line. Another aspect of this 401 MHz band is the approximate three times increase in received Doppler uncertainty. The Doppler processor accommodates this greater search spectrum by increasing its effective frequency cell width from 100 Hz to 1000 Hz. Accordingly, the carrier loop must increase its pull-in range during acquisition to assure carrier lock or sync. Since the cell width is increased by a factor of 10, the analog Doppler correction velocity aid from the Doppler processor must also be scaled-up to properly shift the carrier VCXO to band center at acquisition. Another FET switch varies the scale factor of the Doppler correction into the VCXO summing amplifier to accomplish this.

The carrier track board adjustments are accessible from the top of the board. Normally no adjustment should be required but the procedures are outlined below for reference. Figure 3-13 locates the potentiometers at the top of the board.

- a. ZERO (R45) With receiver in sync apply a digital data clock signal to TP7A and observe the waveform at TP9B using a X1 probe. Adjust R45 for a minimum amplitude square wave.
- b. DOPPLER (R59) Apply a simulated doppler frequency offset by adjusting the MTAR carrier oscillator a chosen number of cps from nominal 10.00 MHz.



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Figure 3-13. Carrier Track Adjustments

Sync receiver then ground TP2A to disable carrier tracking. Measure the frequency of the carrier VCO and adjust R59 for the amount of offset that had been applied to the MTAR carrier oscillator. Return MTAR carrier oscillator to nominal frequency.

c. AGC (R27) With an input signal level of -130 dBm sync receiver and adjust R27 for 1.0 VDC at TP5A.

d. SYNC (R15) Adjust R15 so that sync lamp is on at a signal input level of -133 dBm and goes out with the signal level 1 or 2 dB lower. Note that for each step of the adjustment the signal level should be gradually decreased from a relatively high level. Allow time for the AGC to settle after each level change.

e. Q OFFSET (R78) With receiver in sync and digital data being sent, adjust R78 to zero out any digital data waveform observed at TP8A. Use a X1 oscilloscope probe.

3.2.2.4 Doppler Processor (Four Boards)

The Doppler processor is used in the multimode transponder to perform a Doppler frequency search in an accelerated time over a Doppler uncertainty range. The ranges to be covered are: 4 kHz at 100 Hz per step, which is operated in the 100 bit-per-second or 300 bit-per-second data mode, and the 16 kHz at 1000 Hz per step, which is operated in the 1 kilobits-per-second and higher data mode. The Doppler processor provides a correctional voltage to the carrier and code tracking loops to aid in initial phase-lock acquisition. A simplified block diagram is shown in figure 3-14.

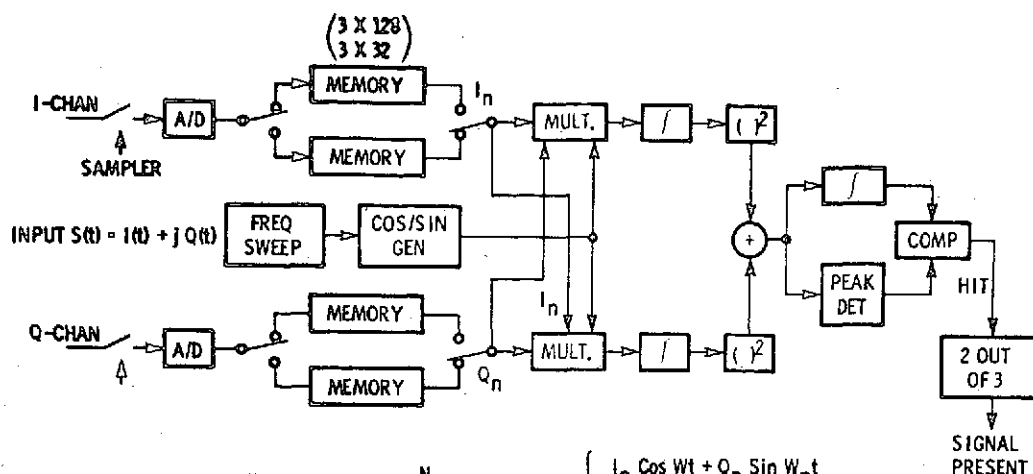
a. Mathematical Formulation

The pulse of unknown frequency can be represented as

$$P(t) = A \cos \left[(\omega_c + \omega_a)t + \theta \right] \quad 0 < t < T$$

where ω_c is the nominal center frequency and ω_a is unknown, uniformly probable over the range $\pm 2\pi W$. Assume WT to be an integer, M ; if necessary by over estimating W slightly.

The first step in the process is to bandpass filter the signal plus noise using a filter of bandwidth $2W$ centered at $\omega_c/2\pi$ Hz. The principal operation next performed is the computation of the Fourier coefficients of the filtered signal plus noise on the interval $(0, T)$. In particular, it is desired to compute the power in each



$$\int_0^{NT} S(t) e^{-j\omega t} dt = T \sum_n S(nT) e^{-j\omega nT} = \begin{cases} I_n \cos \omega t + Q_n \sin \omega t \\ -I_n \sin \omega t + Q_n \cos \omega t \end{cases}$$

- CASE I: 100 BPS ($\Delta F = \pm 4$ KHz)
SAMPLE SIZE (NT) = 10 mS
FREQ. RESOLUTION = 100 Hz (80 FREQ SLOTS)
- CASE II: 1000 BPS ($\Delta F = \pm 12$ KHz)
SAMPLE SIZE (NT) = 1 mS
FREQ. RESOLUTION = 1 KHz (32 FREQ SLOTS)

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Figure 3-14. Doppler Processor

component corresponding to frequencies in the filter passband. These quantities are the values of C_n^2 where

$$C_n = \frac{1}{T} \int_0^T f(t) \exp(-j2\pi n/T) dt$$

for values of n in the region $\frac{\omega_c T}{2} \pm \omega T$.

Alternatively, C_n^2 can be obtained through

$$C_n^2 = a_n^2 + b_n^2$$

$$a_n = \frac{1}{T} \int_0^T f(t) \cos 2\pi n t/T dt$$

$$b_n = \frac{1}{T} \int_0^T f(t) \sin 2\pi n t/T dt$$

In the mechanization it is necessary to store $f(t)$ (which is $P(t) + \text{noise}$) at the filter output. This is conveniently done by resolving $f(t)$ into its quadrature components, sampling and quantizing so that digital memory can be used. The quadrature components of $f(t)$ with respect to a carrier at ω_c are $f_c(t)$ and $f_s(t)$ such that

$$f(t) = f_c(t) \cos \omega_c t + f_s(t) \sin \omega_c t$$

where

$$f_c(t) = A \cos (\omega_a t + \theta) + n_c(t)$$

$$f_s(t) = -A \sin (\omega_a t + \theta) + n_s(t)$$

in which n_c and n_s are independent Gaussian noise processes of zero mean, the same power, both bandlimited to the frequency interval $(-W, +W)$. On the basis of sampling theory, it would be adequate to sample f_c and f_s at the rate of $2W$ samples per second, however, as a practical matter sampling should be at $3W$ to $4W$ samples per second to allow for non-ideal filtering and to improve the accuracy of the numerical approximations to the integrals. Call the actual sampling rate R , such that RT is a convenient integer. Amplitude quantization of the samples can be performed as crudely as one bit, however, this entails a loss of nearly 2 dB in the output signal-to-noise ratio. The use of 3-bit (8-level) quantization reduces this loss to a few tenths of a dB. The sampled, quantized values of $f_c(t)$ and $f_s(t)$ will be represented by $F_c(m/R)$ and $F_s(m/R)$ where the range of the integer m is 1 to RT corresponding to the range of t : $0 < t < T$.

Before writing a final expression for a_n and b_n , it is useful to note certain symmetries in the expressions for values of n spaced equally above and below the midband value, $\omega_c T/2$. To make these evident, let $n = k_c + k$ where $k_c = \omega_c T/2\pi$. The range of k which is of interest is $\pm WT$. Making these changes in notation, approximating $f_c(t)$ and $f_s(t)$ by their sampled, quantized counterparts, and approximating the integrals by sums, we obtain:

$$a_{\pm k} = \frac{1}{2RT} \sum_{m=1}^{RT} F_c\left(\frac{m}{R}\right) \cos \frac{2\pi k m}{RT} \pm \frac{1}{2RT} \sum_{m=1}^{RT} F_s\left(\frac{m}{R}\right) \sin \frac{2\pi k m}{RT}$$

$$b_{\pm k} = \frac{1}{2RT} \sum_{m=1}^{RT} F_s \left(\frac{m}{R}\right) \cos \frac{2\pi km}{RT} \pm \frac{1}{2RT} \sum_{m=1}^{RT} F_s \left(\frac{m}{R}\right) \sin \frac{2\pi km}{RT}$$

Having computed the 2WT pairs of coefficients, a_k and b_k , the 2WT coefficients C_k^2 are formed. Since only one signal is sought, it is the maximum of all the C_k^2 which need be compared to a threshold to make the detection decision. Since the threshold setting should be proportional to the noise power, it may be convenient to set the threshold as a fixed fraction, β , of the noise power as estimated by the sum of all of the C_k^2 . In the usual manner β is chosen to achieve a given false alarm rate, or a given detection probability for a given signal-to-noise ratio, or some similar basis.

b. Mechanization

The computation of a_k and b_k are performed in two modes:

1. $R = 12,800$ sample per second, $T = 10$ ms, and k ranges from -39 to +40. This is equivalent to having 80 filters each 100 Hz wide to cover the frequency uncertainty of ± 4 kHz.
2. $R = 32,000$ samples per second, $T = 1$ ms, and k ranges from -15 to +16. This is equivalent to having 32 filters each 1 kHz wide to cover the frequency uncertainty of ± 16 kHz.

In the following only mode 1 is described since 2 is operationally identical to 1.

The first section of the mechanization is concerned with obtaining and storing the F_c and F_s data. The F_c and F_s signals are the I and Q channel outputs, respectively, from the baseband signal processing module. These signals are converted to 3-bit words and sampled at the rate of 12,800 samples per second. Thus, for $RT = 128$, a batch of data characterizing the signal over 10 milliseconds is obtained (i.e. 128 words each of 3 bits). The memory is of shift register type and consists of four 128-word x 3-bit sections, 2 for F_c and 2 for F_s . The two memory registers for each signal component are organized such that while one memory register is being loaded (gathering new data), the other is recirculating at accelerated rate for processing (computing a_k and b_k). The recirculating rate is 1,024 kHz so that 80 pairs of a_k and b_k are computed in 10 ms, which is the required time interval to gather a new batch

of data by the other memory register. Thus, by alternating the two memory-register's functions, input signals are continually processed until the unknown frequency is found.

The computation of a_k and b_k requires the multiplication of data samples, $F_c(\frac{m}{R})$ and $F_s(\frac{m}{R})$ by the sine and values, $\cos(\frac{2\pi km}{RT})$ and $\sin(\frac{2\pi km}{RT})$ and summing the products. $F_c(\frac{m}{R})$ and $F_s(\frac{m}{R})$ are read out serially from the circulating memory register. The arguments for the sine and cosine are generated by decoding the 4 most significant bits of a 7-bit accumulator which starting at zero accumulates the value of k as m indexes from 1 to 128. (k increments each time m cycles until k ranges from -39 to +40.) At the end of the computation for a particular k , (i.e. at $m = 128$) the $C_k^2 = a_k^2 + b_k^2 \simeq (\sum R_m)^2 + (\sum J_m)^2$ is obtained and is presented to the "auctioneer". This is a register and comparator arrangement which is preset to zero at the start of each data batch and thereafter compares the present content of its register with the newly computed C_k^2 . Whichever is greater is then stored in the register. Thus, at the end of a k cycle (i.e. as k goes through the range from -39 to +40), the greatest value of C_k^2 seen is left in the auctioneer. A final comparison is then made with β times the sum of C_k^2 , which is accumulated in a separate register, to make the detection decision.

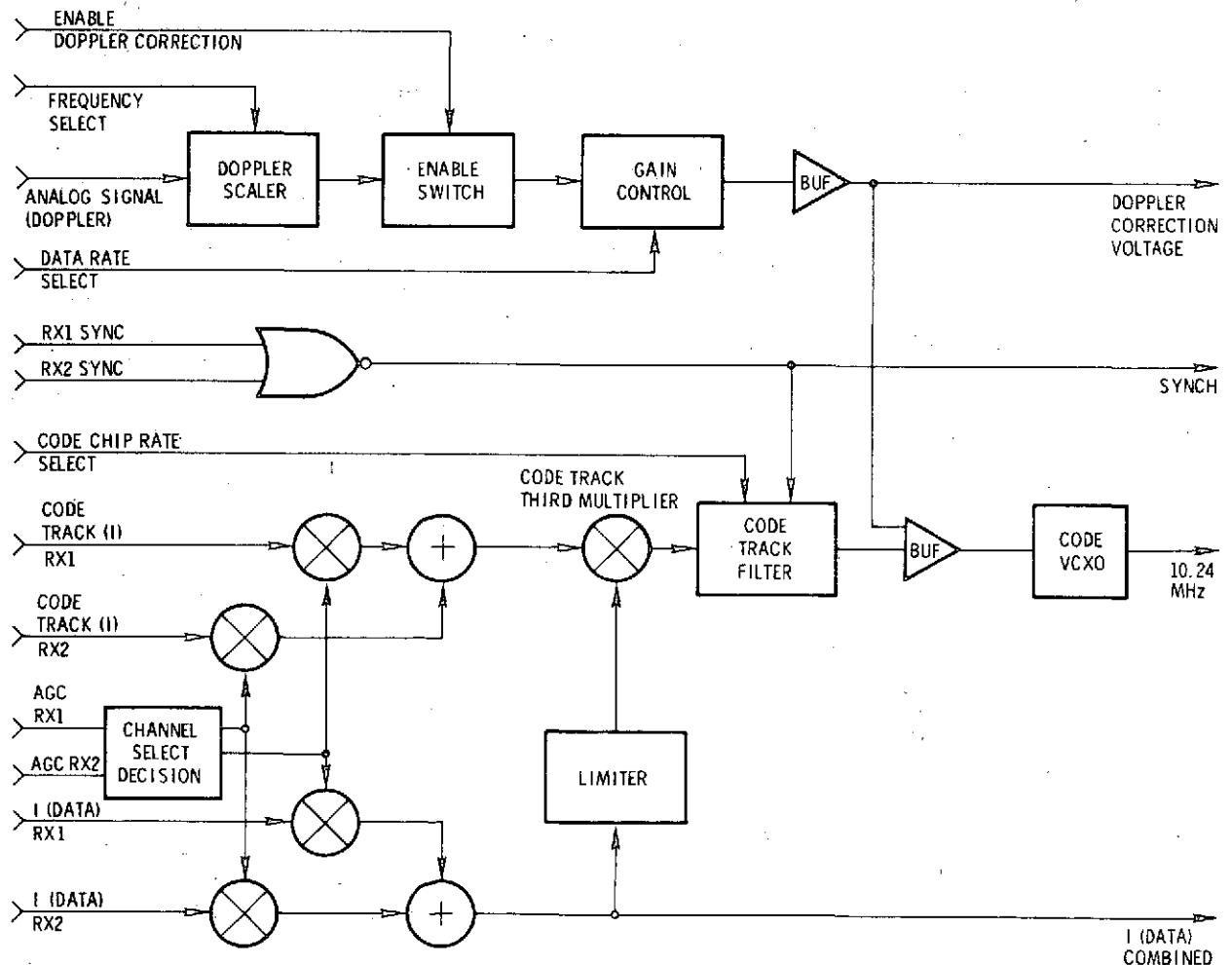
Having detected the presence of a signal as the Doppler processor scans the frequency range in one pass, the doppler processor employs a further decision strategy, whereby two out of three consecutive detections, called hits in the block diagram, are required to be declared a valid hit. This increases the true detection probability and decreases the false-alarm rate under the threshold condition of 10-dB signal-to-noise ratio in 100 Hz. At the conclusion of a valid hit, an analog voltage corresponding to the detected Doppler frequency is sent to the carrier and code-loop VCO's. This voltage effectively drives the local-oscillator frequency to the input carrier for rapid acquisition.

3.2.2.5 Code Track Board

The code track board contains the code track channel combiner, third multiplier, loop filter and VCXO. Included on this board is circuitry for the $R \times 1/$ $R \times 2$ channel select and I (data) combiner. The analog frequency correction signal from the doppler processor is scaled on the code track board and the resulting doppler correction voltage goes to the code VCXO and the carrier VCXO's for both receivers.

As shown in figure 3-15, the channel AGC voltages for Receiver 1 and Receiver 2 are used to make the channel selection decision. Near threshold, the receiver with the best S/N (6 dB) is selected so that full advantage of diversity reception is taken. In the clear both receivers may be selected. The channel select signals are used to choose the inputs to the code track and data combiners.

The code track third multiplier removes the data transitions from the combined code track I channel signal. Note that the carrier track loop third multiplier for each receiver is located on the appropriate carrier track board. The output of the code track third multiplier drives the loop filter. Actually, four independent loop filters are driven in parallel by the output, with each properly scaled in regard to gain and



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Figure 3-15. Code Track Board Block Diagram

response to complement its particular PN chip rate. Selection of 34.133K, 1.02K or 1.024M chip-per-second PN rate and one spare is provided by a four-input, programmable operational amplifier (PRAM), with commutated output. The reason for varying the augmented DC gain of the loop amplifier for each PN chip rate is to compensate for the loss of open-loop gain due to the increasing $\div N$ of the VCO. This $\Delta \div N$ results from the VCO division process in the clock-frequency synthesizer, from the 10.24 MHz VCO to the selected PN chip rate. The $\div N$ term increases from ≈ 10 , to ≈ 100 and then ≈ 300 to generate the 1, 02 MC/S, 102 KC/S and 34 KC/S PN chip rates respectively. By individually setting the DC gain and rolloff capacitor of each loop amp, the desired 2 Hz tracking bandwidth and 0.7 damping factor is maintained regardless of PN chip rate.

The code track filter output is dumped to zero volts when neither receiver is in sync. For signal acquisition the frequency of the code VCXO is determined by the doppler correction voltage. The doppler correction voltage is derived from an analog signal (DOPCOR) from the doppler processor. This analog voltage is properly scaled for the selected receive frequency. The controller, using the "hit" information from the doppler processor, determines when a valid doppler offset frequency has been measured. The enable doppler correction signal from the controller enables the doppler correction to be applied to the code and carrier VCXO's. The data rate selection logic is used to set the proper DC gain for the doppler range (± 4 kHz or ± 16 kHz) in use.

3.2.2.6 Controller Boards

The MMT controller searches the receiver coder to obtain correlation, detects the 31-bit Legendre sequence in data sent from the MTAR and sends a 7-bit Barker sequence to the MTAR and switches from forced data and chip rate to selected value.

There are two controller boards in both the MMT and the MTAR. Differences in the function of the two boards are enabled by modifications in the chassis wiring between the MMT and the MTAR. The basic functions performed by the controller boards include displaying the status of the system, controlling the operation of the doppler processor and enabling the carrier and code tracking loops to close and synchronize to the received signals. Most of the circuitry of the two boards is involved with the PN mode of operation of the system.

Controller board #1 contains a simple minded computer that actually controls operation of the system along with the read only memory chips that store the program for the computer. This computer really can't perform any computation. It has only four commands that it can execute because it is designed specifically for control applications. The four commands are (1) set or reset one of many output flip-flops, (2) input the state of a particular line to the jump control flip-flop, (3) unconditionally transfer to a relative address and (4) if the jump control flip-flop is set transfer to a relative address. Otherwise continue on to the next command sequence.

Controller board #2 which responds to commands from controller board #1 performs the function of searching the coder in PN mode and it also recognizes the Barker sequence or the Legendre sequence in the incoming data. Chassis wiring determines which recognition signal is sent back to controller board #1. It also contains the gating necessary to override front panel controls upon command from controller board #1.

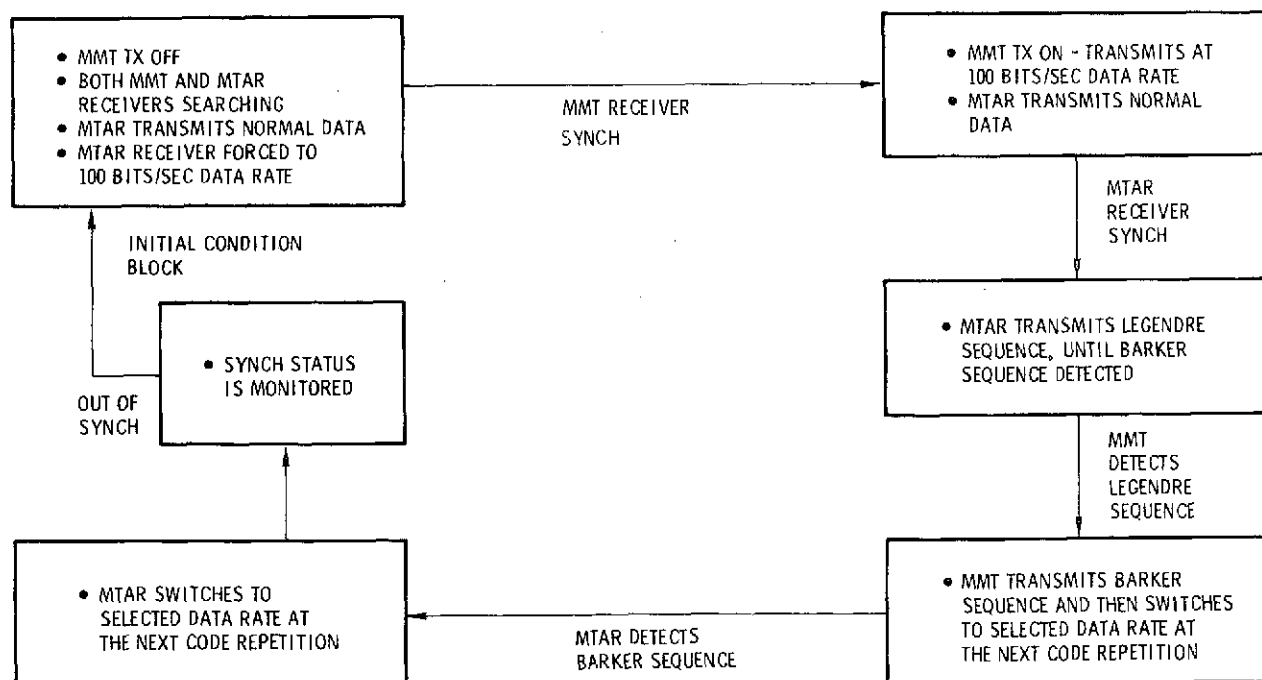
To understand the operations of the controller, a description of the functions performed will be given followed by a simplified flow chart. The actual flow chart used in the design is essentially a program for the controller and confuses the process of understanding basic concepts with many details.

The use of the term MMT standing for Multi Mode Transponder is very appropriate. This system does indeed have many modes of operation and each one has some impact on the controller. There are six basic modes of system operation determined by two front panel switches. One switch selects PN or PSK mode. The other switch selects forward, return, or transpond mode. In addition there are various data rates, coder chip rates, transmitted carrier frequencies, etc. Most of these have relatively little impact upon operation of the controller.

In either PN or PSK mode, the forward and return modes are used for one way operation of the system. Forward and return modes are primarily used for testing purposes rather than simulation of an operational system. Forward mode means that the MTAR transmitter is on continuously and the MMT receiver attempts to lock to the MTAR transmitted signal. The MMT transmitter is left off in this mode. Return mode is just the opposite with the MMT transmitter on and the MTAR transmitter turned off.

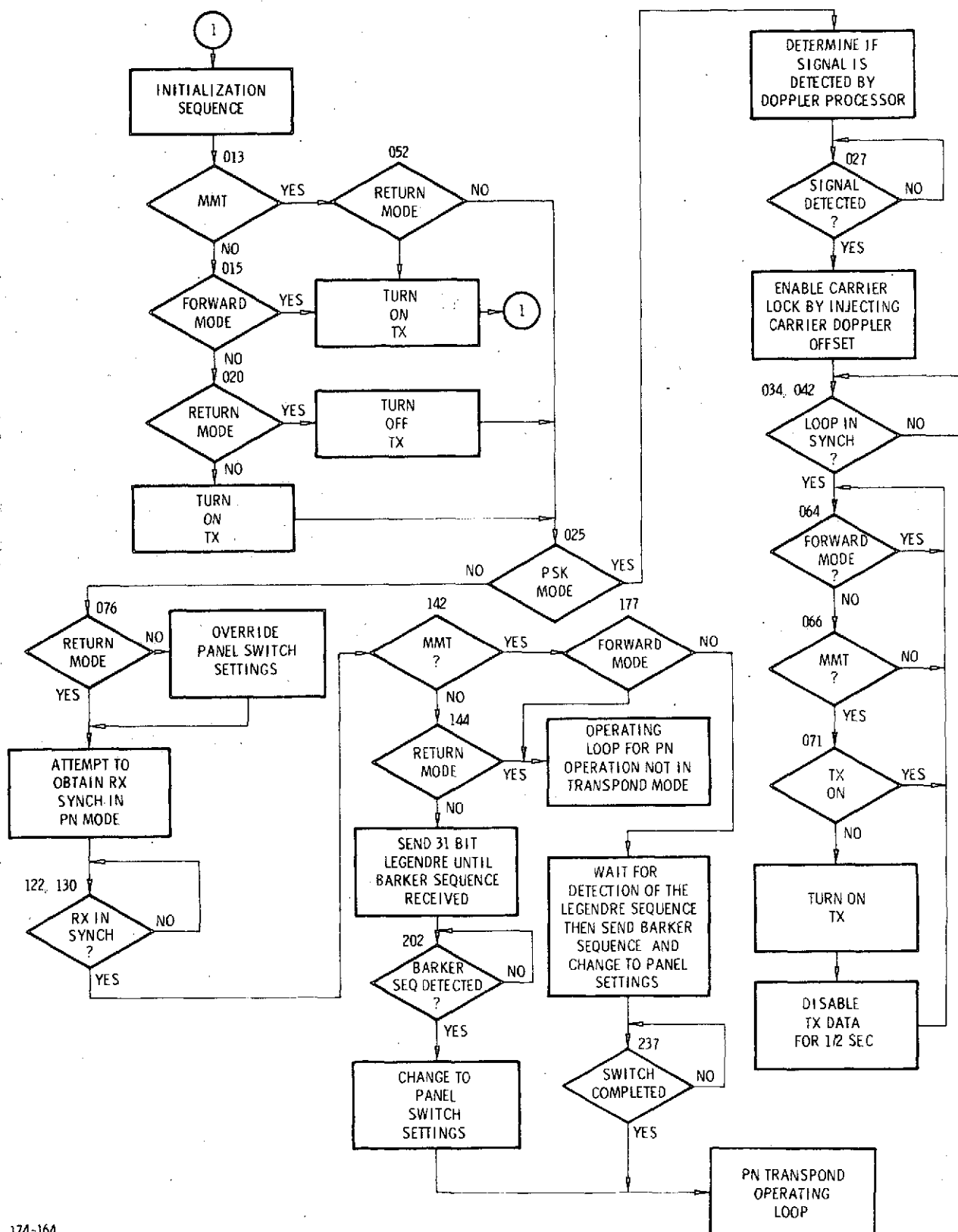
Transpond mode refers to normal mode which simulates a full operational system. PN and PSK transpond modes are fundamentally different as far as the controller is concerned. The operation of PSK transpond mode will be covered in the discussion of the simplified flow chart since it is relatively easy in figure 3-16. This shows the method used to enable rapid establishment of a communications loop which also provides range information. The reason for overriding the return link chip rate is to permit short synchronization times by using the shortest code sequence available. Since the receiver may have to search through all of the code bits in order to obtain correlation and the amount of time necessary to determine correlation doesn't depend upon the coder clock rate a shorter sequence code takes less time to synchronize.

With this brief discussion of the functions performed by the controller completed it is now possible to examine a simplified flow chart, figure 3-17 and see why it does what it does. Starting at point (1) which may always be reached by pressing and releasing the initialize button the controller does just that. It resets various output signals and control flip-flops so that no outputs will be produced from the controller inappropriate to its position in memory. After this initialization the controller determines whether it is an MMT or MTAR and branches in the program as a result of that



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Figure 3-16. PN Transpond Acquisition



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Figure 3-17. Simplified Controller Flowchart

information. It uses a connector pin which is wired to ground in one chassis and left open in the other chassis to determine that fact.

Once the location of the system has been determined, the simplest mode of operation is return or forward modes. In return mode, the transmitter will be turned on if the system is an MMT. Following the path through the decision diamonds indicated by 013 and 052 leads to a spot where the transmitter is turned on and the controller is returned to its starting point. This is also true for the forward mode in the MTAR. This path goes through diamond 013 and 015. The numbers used to identify the diamonds are their location in memory which is displayed on the controller test card if it is plugged into controller #1. When the differences in controller operation between MMT and MTAR are considered it is possible to talk about twelve different controller operating requirements. As shown in the above example, however, there is a symmetry in forward and reverse mode operation because the MMT and the MTAR merely switch places for these two modes. Only transpond mode really requires a special set of program commands to differentiate between MMT and MTAR operation.

The PSK mode of operation is relatively simple compared to PN mode. It does have one peculiarity, however, which is unique to it. The data modulation at the transmit end must be squelched for a short period of time to allow the doppler processor at the receive end to determine the presence of a signal and its doppler offset frequency. This is necessary because the technique of tying the doppler processor sample time to the code repetition used in PN mode is not applicable. Data transmission is stopped for approximately 1/2 second after the initialize button is cycled. Thus, when in forward or return mode, data at the transmitting end is squelched by pressing the initialize button. In transpond mode this same process is used at the MTAR in order to let the MMT synchronize. At the MMT this process is done automatically after the receiver has indicated synchronization.

Referring to figure 3-17, we see that diamond 064 and 066 select the MMT transpond mode (MMT return mode never gets to this point) and the first time through the transmitter will be off. It was turned off after diamond 054. Thus, diamond 071 will be answered no the first time through and the transmitter will be turned on and data squelched automatically. Once the transmitter is on diamond 071 will have a yes answer which will stop the data squelching process.

For the other PSK modes that haven't been discussed yet, operation is basically the same as the transpond mode except that the local transmitter isn't turned on. Forward mode in the MMT and return mode in the MTAR which are the modes not previously discussed are both the same in the sense that the transmitter should be off and the receiver should be looking for a signal. The path through diamond 013 and 052 will turn off the transmitter for the MMT in forward mode. Diamond 064 will prevent the transmitter from being turned on as it must be for transpond mode. The path through diamond 013, 015 and 020 will turn off the transmitter for MTAR return mode. Diamond 066 will prevent the transmitter from being turned on in the PSK operating loop.

As mentioned earlier, PN mode is more complicated than PSK mode. This fact is not obvious in figure 3-17 since many details have been omitted. Diamond 025 leads to PN mode controller operation with the exception of MMT return mode and MTAR forward mode. In these modes the only requirement is to turn on the transmitter and let the code and data rate be selected by front panel switching. The function to be performed for MMT forward mode and MTAR return mode is simply to try and get the receivers into synchronization. Diamond 076 prevents overriding the front panel switch settings for MTAR return mode. In MMT forward mode, the switches always select the code and data rate. The controller can't override the front panel switch setting for the forward mode.

Once the receiver has been synchronized in PN mode for transpond mode in either chassis and forward mode in the MMT or return mode in the MTAR the controller sequence must split again. This process is performed by diamonds 142, 144 and 177. For both the MMT forward mode and the MTAR return mode the operating loop merely monitors the status of the receiver and displays the system status by turning on the ready light. If the receiver falls out of sync, the controller will turn off the ready light and attempt to resynchronize the receiver.

Referring back to figure 3-16, we can see that the MTAR transmits a Legendre sequence to tell the MMT that the MTAR receiver is in synch. Once the MMT detects the sequence it transmits a 7 bit Barker sequence back to the MTAR and both transmitter and receiver in the return link switch to front panel selected rates. The controller sequence to perform this process is different for the MMT and the MTAR. The path through diamonds 142 and 177 in figure 3-17 leads to the transpond sequence for the MMT. The path through diamonds 142 and 144 leads to the transpond

sequence for the MTAR. Once the change to panel switch settings has been made in both the MMT and MTAR they both go to the same PN transpond mode operating loop. This loop monitors receiver synchronization and displays a ready light. If the receiver falls out of sync the controller spends slightly less than a second trying to reestablish synchronization before returning to point 1 (the start of the controller program).

The code and data-clock synthesizer board provides clocks to the coder, the receive data recovery, and the transmit data processor boards. It also supplies a 4KHz clock to the controller boards. The clocks to the coder board are at the actual chip rate while the clock to the TX data processor is four times the front panel selected data rate and the clock to the receive conditioner board is eight times the received data rate. Figure 3-18 shows the synthesis of the data rate clocks and the fixed 4 KHz signal from the 10.24 MHz VCO/XTAL oscillator. Figure 3-19 is a block diagram of the coder clock synthesis. There are three synthesizer boards in the system. By adding some circuitry to the design it was usable in all three different applications.

Figure 3-18. Data Clock Synthesizer

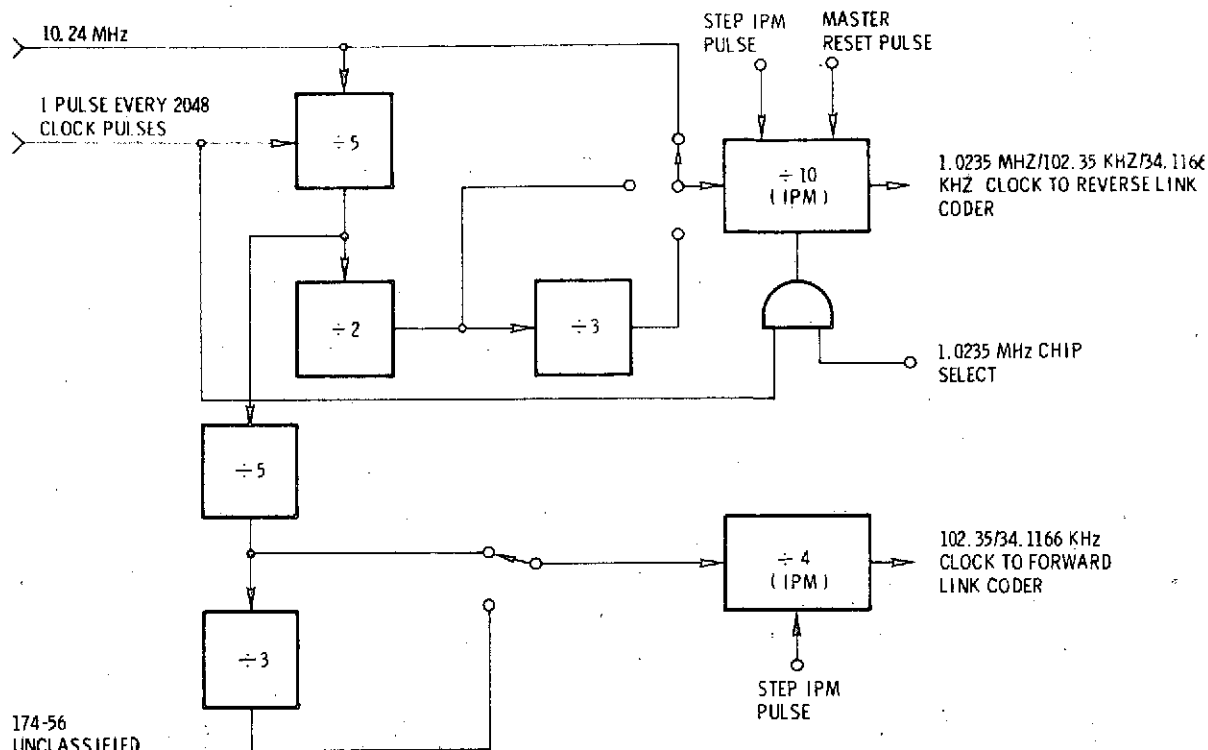


Figure 3-19. Coder Clock Synthesizer

In the MMT the synthesizer board is driven by a 10.24 MHz VCO which is used to track the incoming code phase in PN mode. In PSK mode the VCO input is grounded so that it acts as a stable frequency source. Since the MMT is a coherent transponder, the return link code rate is derived from the forward link received code rate. Therefore, doppler frequency shifts appear at the code clock output. The master reset pulse which originates at the forward link (receive) coder not only resets the data clock countdown chain but the return link coder clock countdown chain so that the phase of the return link coder is exactly the same as the forward link coder. This condition is necessary for round trip range measurement. The master reset pulse also synchronizes the doppler resolver circuitry so that data transitions do not occur in the middle of a sample period. Referring to figures 3-18 and 3-19 again, all of the outputs shown are used in the MMT. The terminology of 8X actual RX data rate and 4X selected data rate is used because the data encoding/non encoding decision is implemented on the TX transmit data processor board. It varies its division factor to compensate for the selection of coding. In the receiver, however, this switching is performed on the clock synthesizer board itself.

In PSK mode the divide-by-4 IPM receives pulses from circuitry on the RX receive data recovery board and varies the phase of the 8X RX data rate clock as a function of these command pulses. The term IPM stands for incremental phase modulator and describes the function performed. It advances or retards the phase of the output signal as a function of command signals. The forward link coder in the MMT is a receiver coder and command signals from controller board #2 are applied to the divide-by-4 IPM on figure 3-17 to search the receive coder looking for correlation.

The return link coder, which is a transmitter in the MMT, doesn't need to be searched. Consequently the divide-by-10 IPM in figure 3-19 doesn't receive any step pulses and merely counts down the input frequency without phase shifting the output frequency.

3.2.2.8 MMT Frequency Synthesizer Boards

Each MMT frequency synthesizer (figure 3-20) consists of two boards which are used to generate the corrected frequencies for use in the MMT transponder. The outputs of the MMT boards no. 1 and no. 2 are specified in table 3-2. A separate frequency synthesizer is used with each of the two diversity receivers.

Table 3-2. MMT Boards Outputs

	Frequency in MHz	Power Level in dBm	Minimum Spur Isolation in dB	Signal Name Use
MMT/MTAR Board No. 1	5.00	TTL Squarwave	N /A	L04-1/2
	60.00	+4 ±1 dB	50 dB	L01C-1/2
MMT Board No. 2	81.25	+4 ±1 dB	50 dB	L01B-1/2
	84.00	+4 ±1 dB	50 dB	L02-1/2
	137.00	+0 ±1 dB	40 dB	TXL0-1/2
	333.25	+4 ±1dB	50 dB	L01A-1/2
	15.00	+4 ±1 dB	40 dB	L03-1/2

a. MMT Board No. 1

Each MMT/MTAR board No. 1 is driven by a 10 MHz squarewave input from its receiver carrier VCO. Of the nine outputs from board No. 1, seven outputs drive board No. 2 and two outputs are local oscillator signals.

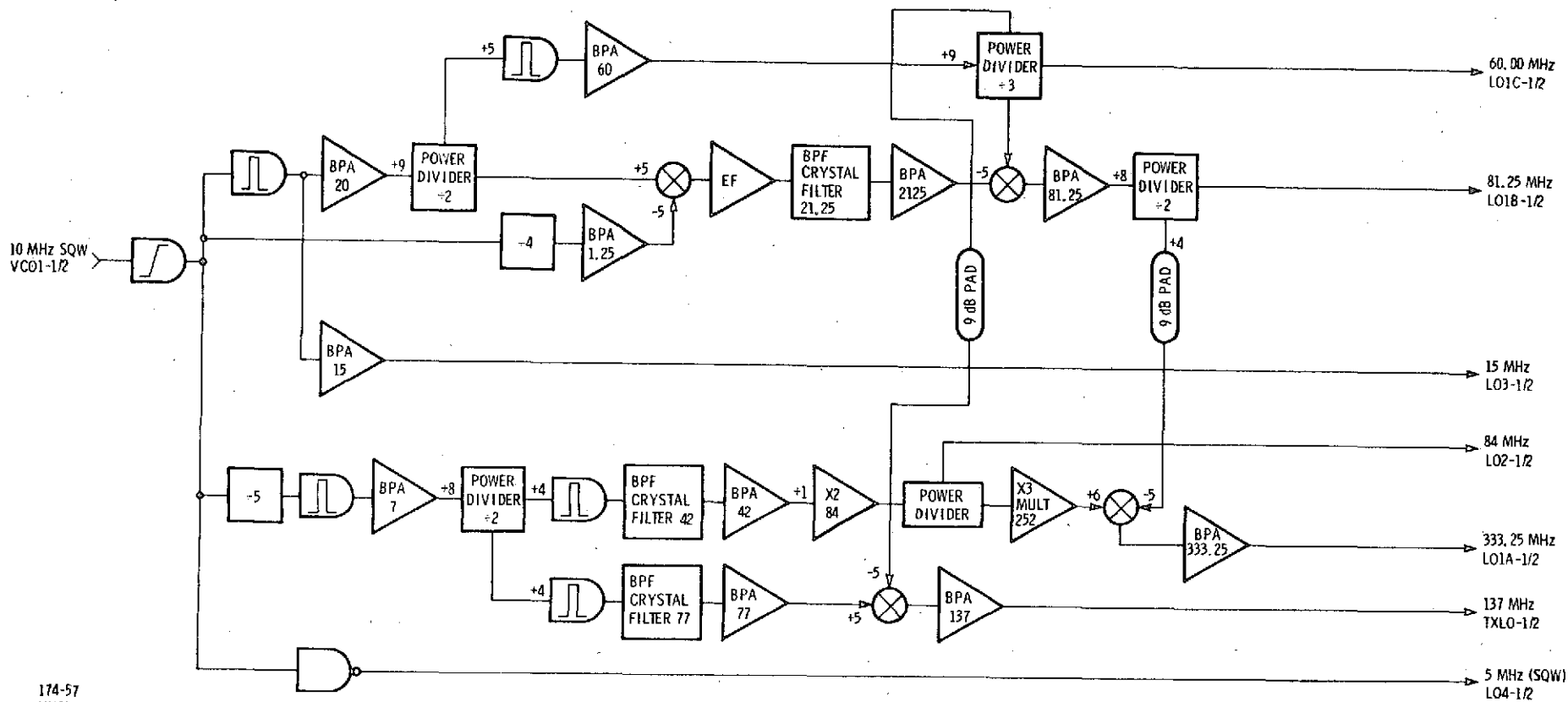


Figure 3-20. MMT Frequency Synthesizer

b. MMT Board No. 2

The MMT board no. 2 supplies the 15 MHz (L03-1/2), the 84 MHz (L02-1/2) and the 137 MHz (TXL0-1/2); it also supplies the outputs 60 MHz, 81.25 MHz (L01B-1/2) and 333.25 MHz (L01A-1).

3.2.2.9 Coder Board

The coder board contains a forward link coder, a return link coder, and ambiguity resolving circuitry to provide range information in the MTAR. Figure 3-21 is a block diagram of a return link coder. The forward link coder is similar but simpler since it only has to handle two chip rates (34 and 100K chips/sec) and it doesn't need restart capability.

The basic concept of the coder is the use of two 11-stage sequence generators to produce two different maximal linear sequences. The outputs of these generators are modulo two added to produce a new sequence. This "Gold code sequence" is the actual one used for PN transmission. Its advantage is that by changing the phase of one of the 11-stage sequence generators with respect to the other one a new Gold code can be produced which will not correlate with the first such sequence produced. This feature allows multiple access use of one satellite

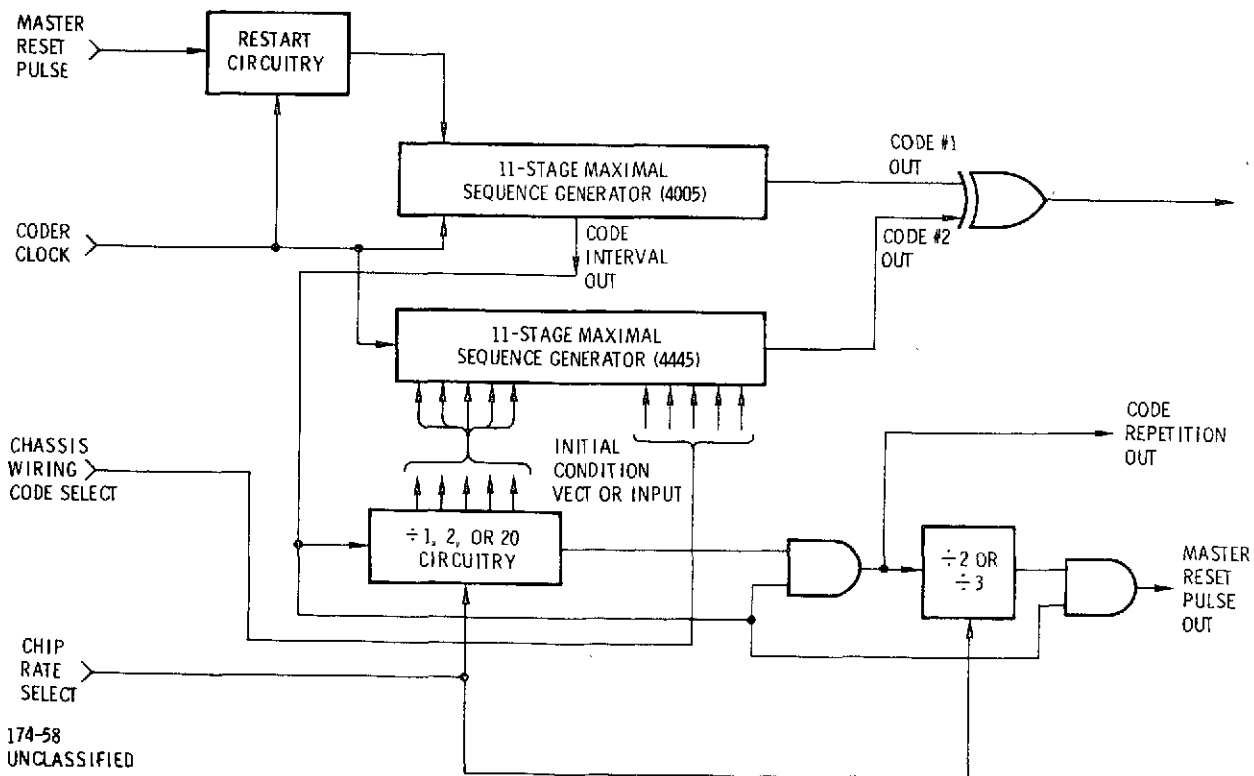


Figure 3-21. Return Link Coder

through code multiplexing with minimum hardware. It is also used to extend the length of the transmitted code for certain chip rates.

The upper 11 stage sequence generator in figure 3-21 has a code incidence detector which uses the all ones state in the generator. This all ones vector will occur only once every cycle of the sequence generated. This code incidence is used to load a vector into the lower sequence generator. At 34 K chips per second, the same vector will be loaded into the lower sequence generator every time. This vector consists of five bits from the divide-by-1, 2 or 20 counter and six bits determined by chassis wiring. These six bits permit modification of the code for test purposes if desired. At 34 K chips per second, the counter is used to "divide-by-1" which means that it is held in the same state all the time and that this state enables the AND gate drawn to the right of the counter. This also insures that the same vector will be loaded into the lower sequence generator every time. With these conditions the output code sequence will have the same repetition as that of the upper sequence generator which is 60 Msec.

When the chip rate is 100K chips/sec, the period of the upper sequence generator becomes 20 Msec. The length of the output sequence is now lengthened to 40 Msec by allowing the divide-by-2 condition in the counter. On alternate code repetitions of the upper sequence generator one of two different vectors is injected into the lower sequence generator to produce the longer code output. When the 1M chip/sec rate is selected the upper sequence generator has a 2 Msec period. The output code sequence is kept 40 Msec long by injecting twenty different vectors into the lower sequence generator. These long code intervals were provided for protection from multipath phenomena.

The divide-by-two or -three counter shown at the bottom of the block diagram serves to generate the master reset pulse (MRP) every 120 ms. This pulse is used for synchronizing the data countdown chains at both ends of a link. It also phases the return link coder to the forward link coder in the MMT. The master reset pulse occurs every second code repetition at 34K-chip rate and every third code repetition (not the upper PNG repetition) at either 100K- or 1M-chip rates. Since at the MMT it is possible to be receiving with a basic repetition rate of either 40 or 60 ms and transmitting at either 60 or 40 ms, some method is needed to phase the return link coder that will not produce code phase jumps once the receiver is locked. By using a

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repetition period of 120 ms which is a common repetition period for all coder chip rates the phasing can be performed continuously without producing transients in the return link coder phase.

This 120 Msec repetition lines up the forward and reverse link coders at the MTAR. There are three possible combinations of coder chip rate that need to be considered for purposes of obtaining round trip range information at the MTAR. If the forward and reverse link codes have the same period the master reset pulse will phase the two codes identically and range information may be obtained merely by measuring the time between a forward (TX) link and a reverse (RX) link code repetition at the MTAR. When the forward and reverse link coder rates are different a meaningful range measurement can be taken every 120 msec. Since one of the periods will be 60 Msec and the other 40 Msec selection of the proper code repetition period must be made. This is done by selecting every second code repetition if it is 60 msec or every third repetition if it is 40 msec.

The ambiguity-resolving circuitry shown in figure 3-22 contains a divide-by-2 and a divide-by-3 circuit which select the appropriate phase of the forward link code repetition. The decoding logic and associated gating use every TX coder repetition in the MTAR to start the range timing process if both forward and reverse link code repetition periods are the same. If the TX period is 60 msec, every second one is used and every third one is used if the period is 40 msec. The RX code repetitions always stop the range counter since the round trip propagation for the test system will be less than 20 msec.

In order to phase the divide-by-2 and divide-by-3 counters a single shot is fired by the start range counter pulse. The period of the single shot is long enough to include the maximum expected round trip range time in the test system. If the receive code repetition occurs during the time slot opened by the single shot the latch which has been reset by the leading edge of the forward link code repetition will be set again. The latch in the set condition allows the two counters to continue cycling normally. If a receive code repetition does not occur during the single shot window it means that the counters are not phased properly. When this happens the latch stays in the reset condition which prevents the counters from cycling normally. The counters will be held in one state until the single shot window coincides with a return link coder repetition. Thus the circuitry automatically phases either the divide-by-two counter for 60 msec TX coder repetition or the divide-by-three counter for 40 ms forward link coder repetitions and removes the ambiguity.

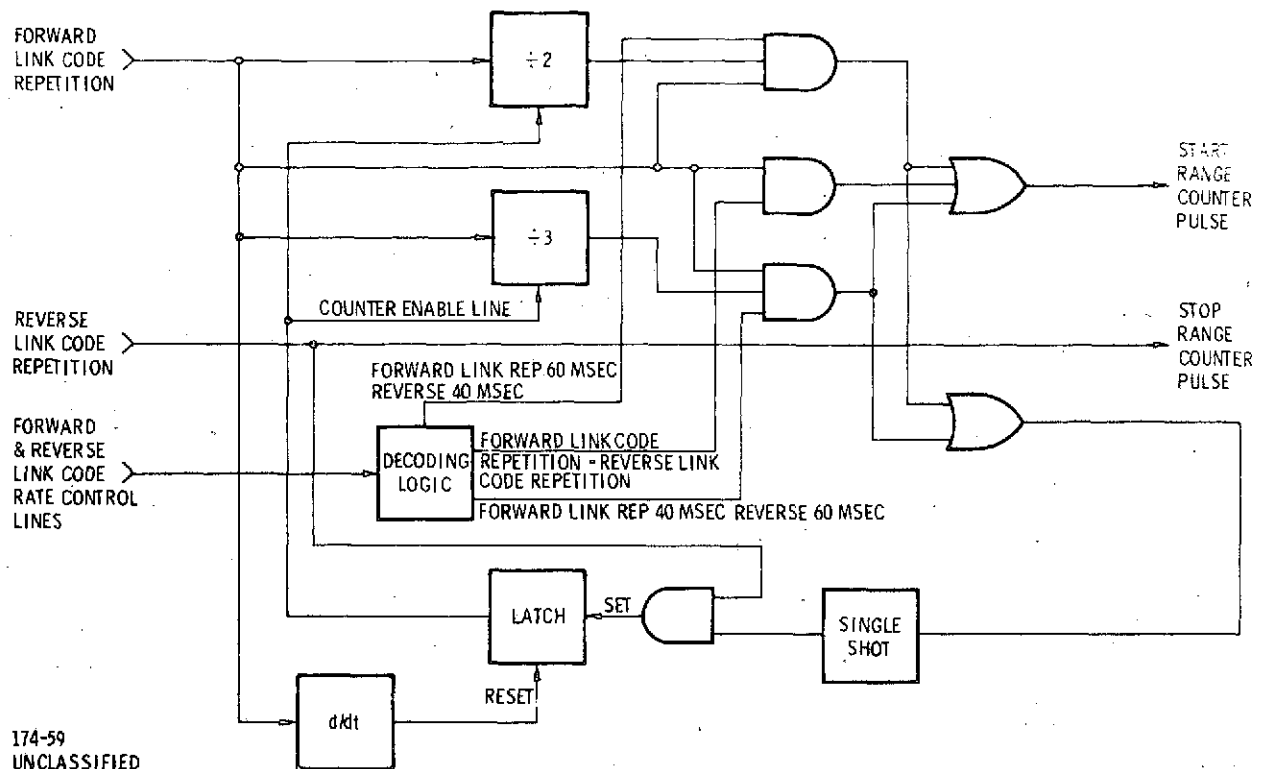


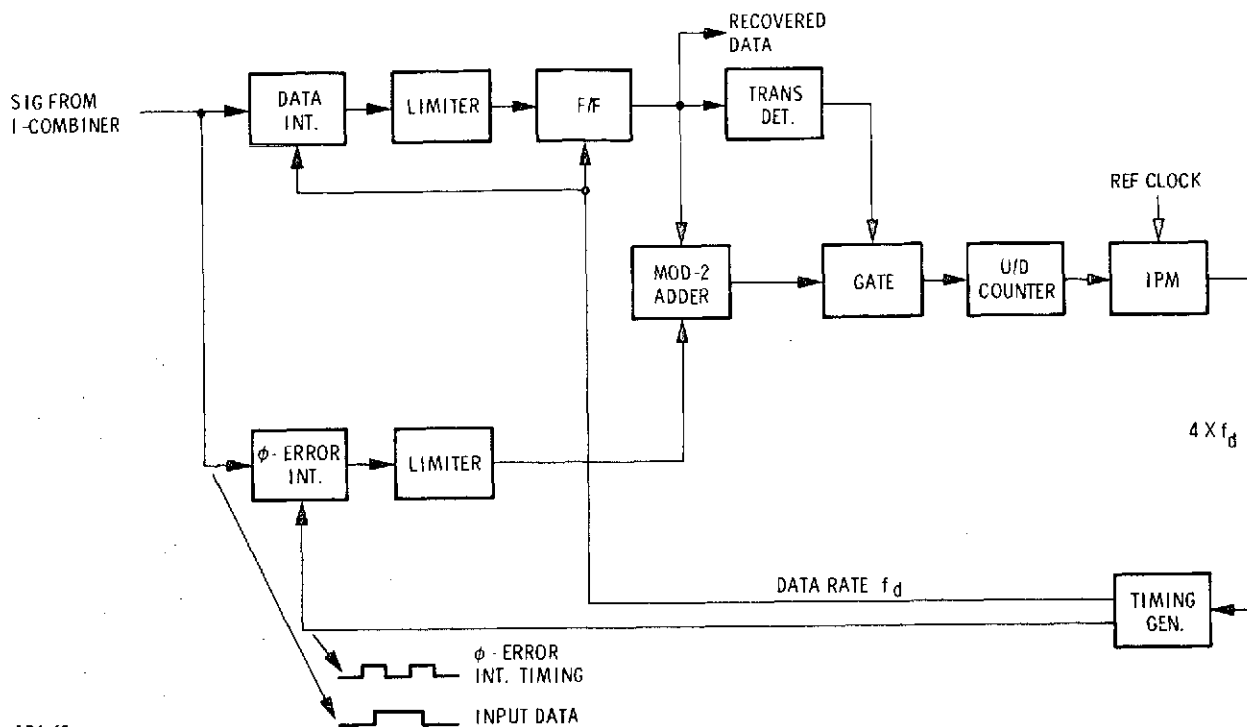
Figure 3-22. MTAR Range Gating Logic

3.2.2.10 Data Recovery Board

The data recovery board contains the circuitry to extract digital data and data clock from the combined I channel signal. The data rate control signals are decoded on the data recovery board for use in switching integration time constants and loop filter bandwidths.

A block diagram of the data clock tracking loop is shown in figure 3-23. All of the blocks shown are contained on the data recovery board except the incremental phase modulator. The IPM circuitry is part of the code and data-clock synthesizer board.

The input signal to the data integrator and phase error integrator is the combined I-channel outputs of the two diversity receivers and is in NRZ format. The data integrator performs the function of matched-filter detection by integrating the received signal over the full bit time. At the end of each bit, the integrated value is sampled and a hard decision made to determine the data. The recovered data is then stored in flip-flops to be used in a modulo-2 adder and transition decoder.



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Figure 3-23. Data Clock Tracking Loop

The phase error integrator "sniffs" around the bit edges for tracking error signal. Its integrated time is $1/2$ bit and covers the last and first quarters of adjacent bits. At the end of each integration time, the integrated value which represents the tracking error is sampled and quantized to one bit (+ or -). The quantized signal is then modulo-2 added to the recovered data to obtain a binary signal whose value depends on whether the local bit phase is leading or lagging the received bit phase.

Since in NRZ data format, valid error signal exists only when there is data transistion, the binary error signal is gated through to the U/D counter by the transistion Detector. Data transistions are detected by simply modulo-2 adding the recovered data stream with a $1/2$ bit delayed version.

The U/D counter functions as a smoothing filter for the error signal. It counts the + or - pulses at each data transistion time until it reaches ± 8 , at which time a pulse is sent to the incremental phase modulator (IPM). The IPM is actually a variable modulo counter with a normal cycle of 100 count. When the U/D counter overflows or underflows, the IPM changes to modulo-99 or modulo-101, respectively, for one counting cycle and then reverts back to modulo-100. This has the effect of shifting the local bit phase at $\pm 1/100$ of a bit.

The IPM output which is at 4 times the data frequency is next divided by 4 in the timing generator to yield the various timing signals at the data rate for operation of the data integrator and phase error integrator, thus effectively closing the clock tracking loop.

Although the nominal signal-to-noise ratio, E_b/N_o , at which the loop is expected to operate, is greater than 7dB (i.e. usable data of 10^{-3} bit error rate or less requires E_b/N_o greater than 7dB), it is desirable to design the loop with margin so that tracking error does not contribute significantly to bit error in the demodulation process. Consequently, the U/D counters boundary is set at ± 8 . This effectively sets the closed loop bandwidth at 6×10^{-4} times the data rate f_d for $E_b/N_o = 0$ dB, resulting in tracking error less than 0.02 bits.

Since the maximum doppler due to satellite motion is on the order of 30 PPM (i.e. 12 KHz at 400 MHz), and since the transmitter data clock stability is better than 10 PPM, the maximum frequency offset to be tracked by the receiver's data clock tracking loop is less than 50 PPM. The loop is of first order type, which will have a steady-state tracking error due to the frequency offset. However, this error is roughly 0.02 bits at $E_b/N_o = 0$ dB and is considerably less for $E_b/N_o = 7$ dB. That is, at high E_b/N_o , the loop can track frequency offset Δf , of approximately 625 PPM. i.e.

$$\begin{aligned}\Delta f &= \left(\frac{1 \text{ pulse}}{8 \text{ bit}} \right) \left(\frac{f_d \text{ bit}}{2 \text{ sec}} \right) \left(\frac{1}{100} \frac{\text{bit}}{\text{pulse}} \right) \\ &= \left(\frac{1}{1600} \right) (f_d)\end{aligned}$$

Which is greater than the expected doppler. Therefore, a first order loop as designed will suffice for the present application.

3.2.2.11 MMT/MTAR Modulator Board

The MMT modulator board has two modes of operation:

- a. PN Mode - The data to be transmitted is first modulo-2 added to a PN code. The resulting signal then balance-modulates a 137 MHz carrier to generate a PSK, spread spectrum signal for transmission.
- b. Conventional PSK Mode - Digital data balance-modulates the selected 137 MHz carrier.

The MMT/MTAR modulator board is used in both MMT and MTAR. The configuration is changed by moving two RF cable connectors located on the board. Figure 3-24 is a block diagram of the MMT configuration. The transmit on/off control comes from the controller. In transpond mode the MMT does not transmit until one of the diversity receivers is in sync with the signal from the MTAR. The output of the modulator board drives the power amplifier located in the RT chassis.

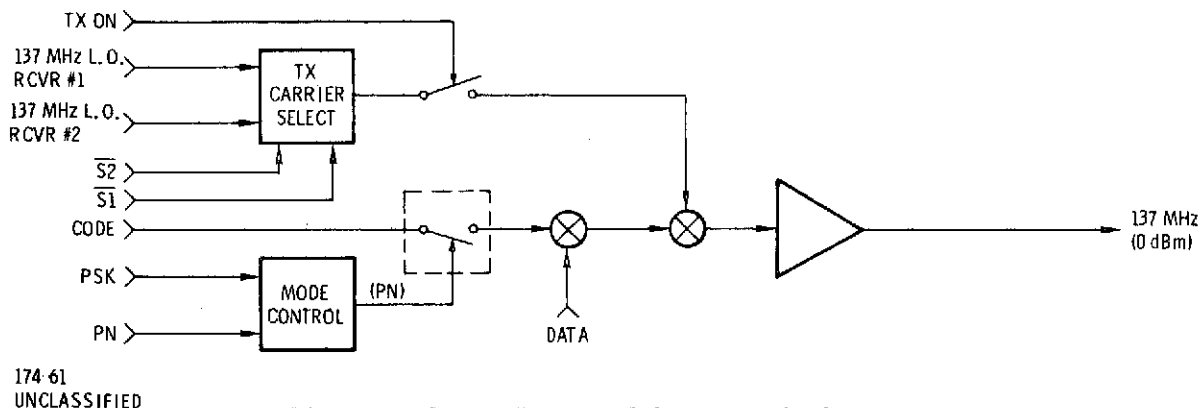


Figure 3-24. MMT Modulator - Block Diagram

To select the carrier signal for transmission from the two diversity receivers, the switching logic signals from the diversity combiner are used. The selection is as follows:

<u>S₂</u>	<u>S₁</u>	<u>Carrier Selected</u>
1	0	RCVR 1
0	0	RCVR 2
0	0	RCVR 2

Selection of RCVR No. 2 carrier for $S_2 = 0$ and $S_1 = 0$ is entirely arbitrary, for under this condition both carriers are equally usable and RCVR 1 could have been selected instead.

3.2.2.12 PDM Voice Board

The suppressed-clock PDM demodulator waveforms are shown in figure 3-25. A Costas loop tracks the suppressed PSK carrier and synchronously demodulates the PDM carrier. The recovered SC PDM signal is modulo-2 added with the 10-kHz PDM clock divided by 2.

The recovered PDM signal is processed (see figure 3-26) by an integrate-and-dump filter which makes the optimum estimation of the transmitted signal. The sample-and-hold circuit remembers the final value of the integrate and dump circuits (i.e., immediately before the integrator is dumped). The output of the S and H is the

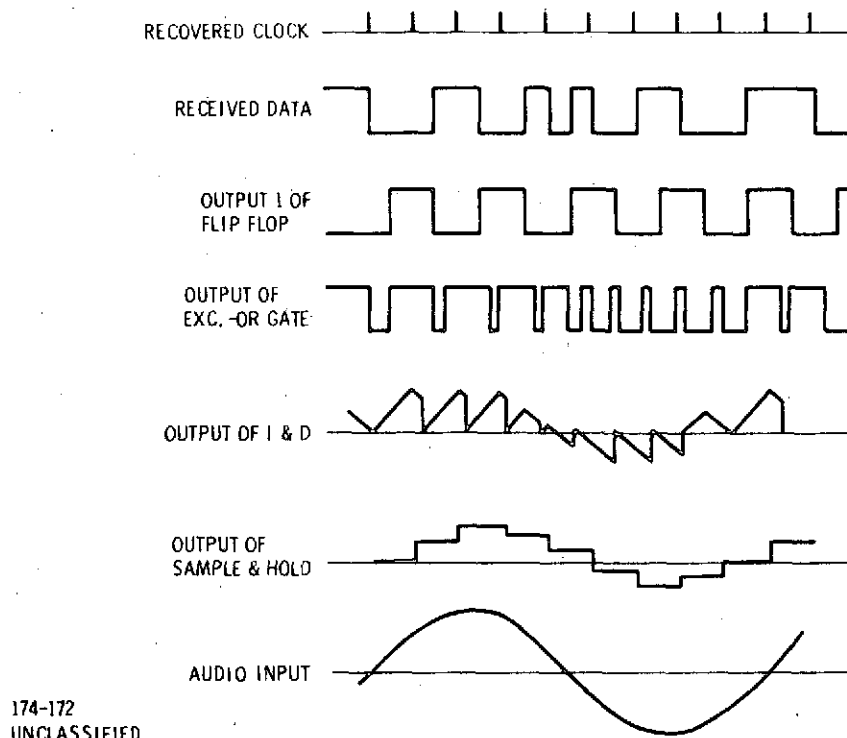


Figure 3-25. Demodulator Waveforms

recovered audio in a PAM format. The PAM signal is processed by the voice conditioner which provides deemphasis, low-pass filtering, and buffering into a 600-ohm line and a headset output.

It should be noted that the critical aspect of the total demodulation process is the acquisition of the clock and its insertion in proper phase. This process is inherent in a PN system since the PDM clock is generated from the above source on the PN code clock. As long as PN correlation is maintained, a phase coherent PDM clock is available for PDM demodulation.

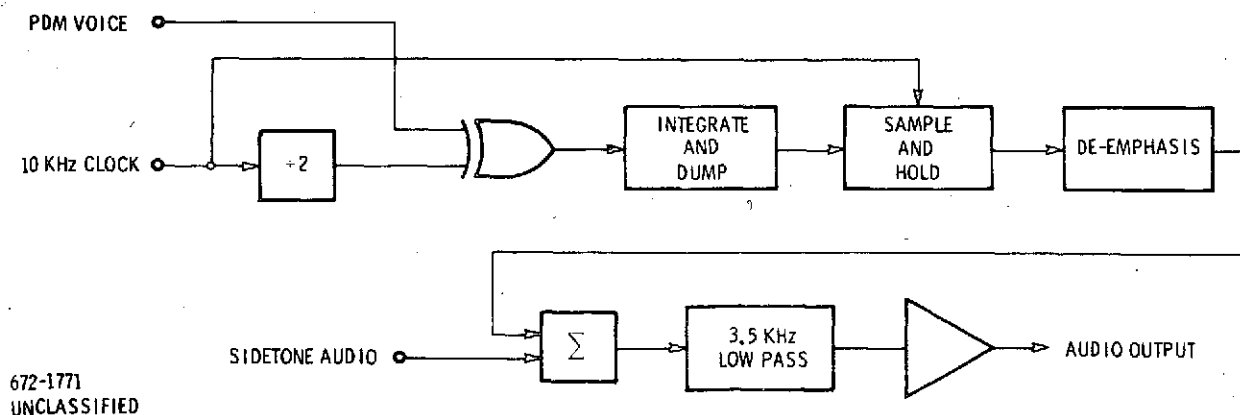


Figure 3-26. Suppressed Clock PDM Voice (Receive) - Block Diagram

A block diagram of this suppressed clock PDM modulator is shown in figure 3-27. Speech conditioning consists of a preemphasis network, AGC, a compressor and a 3.5-kHz lowpass filter. The audio AGC circuit ensures a high index of modulation while the compressor increases the effective modulation.

A sample-and-hold circuit takes very short samples (1 microsecond) and holds them for a sample period. A ramp generated from the 10 kHz clock and a comparator constitute the PDM modulator. The modulo-2 addition of PDM and 5-kHz squarewave removes the clock transitions from PDM and results in suppressed carrier PDM.

The audio input signal is transformer-coupled into a preemphasis network. The audio preemphasis increases the gain at a 6-dB-per-octave rate between 600 Hz and 3500 Hz.

The pre-emphasized audio is followed by the AGC amplifier, from which the signal is fed into the speech-compressor clipper. The speech-compressor output goes through the 3.5-kHz, low-pass filter. This active filter provides a five-pole Legendre response with a 3-dB point of 3710 Hz and 20-dB relative attenuation at 5 kHz.

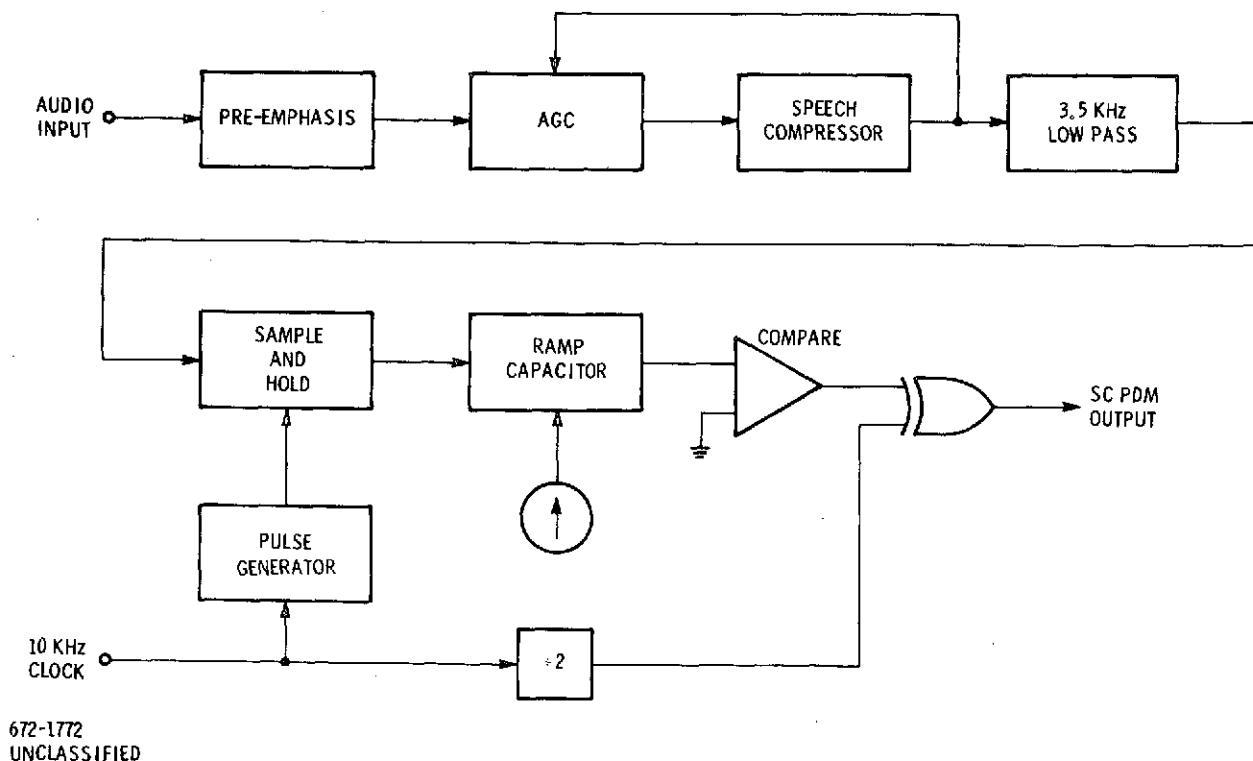


Figure 3-27. Suppressed Clock PDM Voice (Transmit) - Block Diagram

The maximum low-pass filter output is approximately 4.0 v p-p, centered at -2.00 Vdc. This offset is required for proper PDM modulator operation.

The AGC amplifier provides constant output signal (± 1 dB) for any input signal between 80 mV RMS and 1V RMS, providing a 22 dB AGC range. For applications in installations with high ambient noise, the audio input level control is adjusted to set the background noise level at least 6 dB below the AGC threshold. The AGC time constants are set for nominal attack and release times of 100 ms and 2 seconds respectively.

The speech processor output drives a sample and integrate circuit. The audio is sampled at a 10-kHz rate and the samples are applied to a capacitor which is also driven by a constant current source. The audio samples always result in negative voltages between 0 and -4V on the capacitor. The constant current source then pulls the capacitor back above ground. A comparator switches state each time the capacitor voltage crosses zero. The time interval between negative and positive zero crossings is a linear function of the input signal, generating a pulse-duration-modulated (PDM), 10-kHz subcarrier. A -2.00V pre-bias of the low-pass filter output ensures that the PDM output is a squarewave if no audio is present.

A 5-kHz clock, derived from the input 10-kHz clock by division, is modulo-2 added to the PDM signal. This process removes the stationary, redundant clock edges from the PDM, producing the suppressed clock pulse duration modulated (SCPDM) signal.

Figure 3-28 shows the waveforms at each significant point in the PDM modulator, assuming a single tone at the input. The input audio is sampled and held, and compared with a sawtooth signal generated from the sampling clock. The comparator output is a pulse-duration-modulated (PDM) clock signal. The regular recurring (rising) edges of the PDM waveform are suppressed by modulo-2 addition with the half-clock signal. The resultant SCPDM binary signal keys 180-degree phase-shift modulation of the output IF carrier.

3.2.2.13 Transmit Data Processor Board

The TX data processor board contains the convolutional encoder circuitry, digital data clock countdown, and modulator data control. The TX data processor board also includes the lamp drivers for the control panel displays.

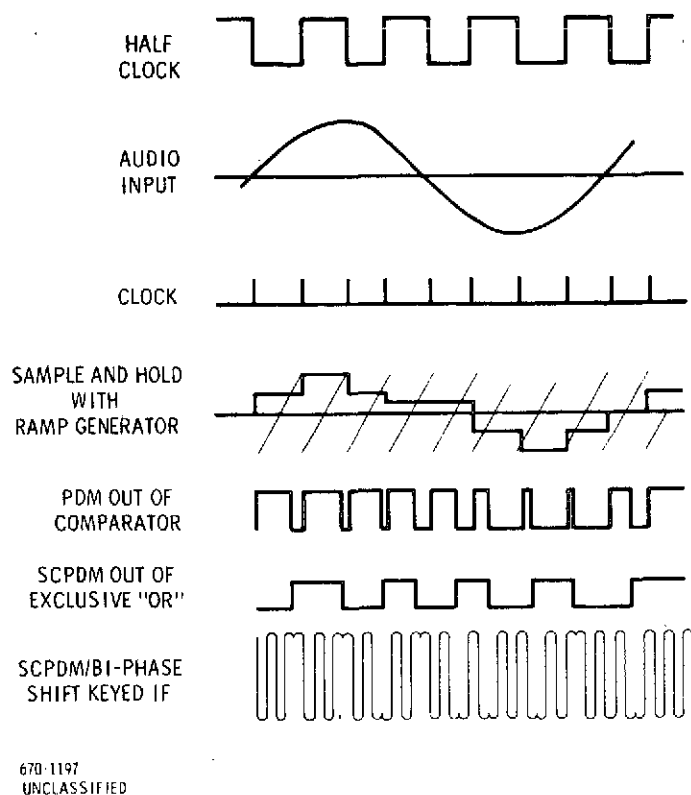


Figure 3-28. PDM Modulator Waveforms

The convolutional encoder function in the MMT was designed to transform a digital information sequence k into some longer output sequence such that the GSFC decoder can uniquely and with arbitrarily high probability redetermine the k in spite of binary symmetric channel perturbations. The design goal was to achieve a bit error probability of 10^{-5} at an E_b/N_o of 4 dB. The specifications are listed in figure 3-29.

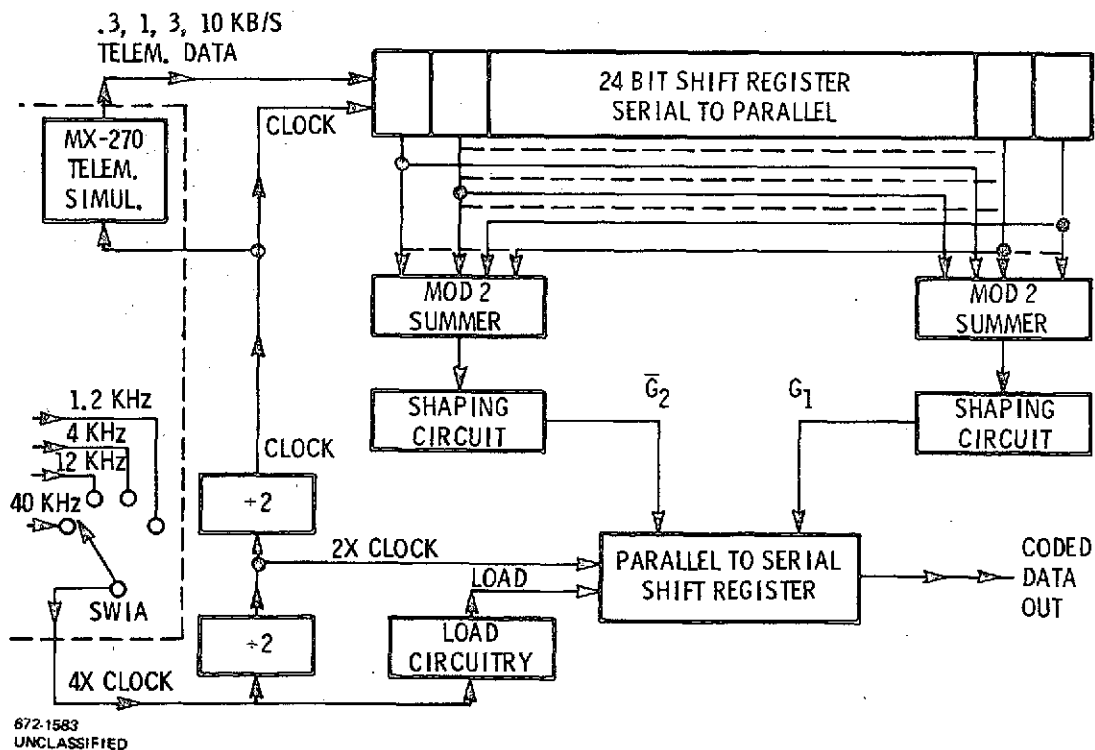
The 24-bit, serial-to-parallel, shift register shown in figure 3-30 consists of three, 8-bit shift registers connected in tandem. The boolean expression for the two modulo-2 summers obtained from the parity generator codes will have the form, $A \oplus B \oplus C \oplus \dots$. The shaping circuits are J-K flip flops used to clean up any switching spikes in parity bit streams G1 and G2.

ENCODER RATE	1/2
CODE TYPE	NON-SYSTEMATIC
CONSTANT LENGTH	24 BITS
CODE	$g_1 = 73353367$ $g_2 = 53353367$
FRAME LENGTH	2047 BITS - ENCODER INPUT 4094 BITS - ENCODER OUT
FRAME SYNCHRONIZATION CODE	ENCODER INPUT 16 BITS 604324 ENCODER OUTPUT 32 BITS 77264244734
FLUSH CODE (ENCODER DUMP)	ENCODER INPUT 24 BITS 11702625
BIT RATES	ENCODER OUTPUT .6, 2, 6, 20 KB/S
QUANTITIZATION	TO BE DONE BY DECODER

NOTE: ALL OCTAL DIGITS SHOWN IN ORDER OF INCREASING TIME;
THE OLDEST DIGIT IS ON THE LEFT.

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Figure 3-29. Specifications-Convolutional Encoder



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Figure 3-30. Block Diagram Convolutional Encoder Board

The frame length at the input to the convolutional encoder was chosen equal to that of the telemetry simulator (MX-270), which provides a 2047-bit PN sequence. The frame length is defined as the sum of the flush-code bits, synchronization-code bits, and data bits. The flush code is used by the sequential decoder for reinitialization, and must be equal to the constraint length of the encoder. Therefore, the flush code at the encoder input will be 24 bits, and the synchronization code was selected to be 16 bits. The 24-bit flush code will generate 48 parity bits at the output of the encoder, and will be followed by a 16-bit synchronization which will generate 32 parity bits at the output of the encoder. The input flush and synchronization codes are contained in the PN sequence generator as 40 consecutive bits (24 flush bits + 16 synchronization bits). The frame synchronization code and flush code are shown in the specification chart in figure 3-29 in octal form.

3.2.3 CONTROL BOX

A remote control box is provided for the MMT. Front panel switches and indicators are provided to facilitate mode selection for the experiments to be performed.

The following selector switches are provided on the MMT control Box.

- Link Mode - Forward only
Transpond
Return only
- Modulation Mode - PSK
PN

Forward Link

- PN Chip Rate - 34.133 K chip/s
102.4 K chip/s
- Data Rate - 100 bits/s
300 bits/s
1000 bits/s
Voice
- Frequency - 127.75 MHz
149.0 MHz
401.0 MHz

Return Link

- PN Chip Rate - 34.133K Chip/s
102.4K Chip/s
1024K Chip/s
- Data Rate - 0.3K Bit/s
1.0K Bit/s
3.0K Bit/s
10.0K Bit/s
Voice
- ⊙ Data Encode - On
Off

A margin to threshold meter scaled in dB is provided for each of the two diversity receivers.

3.2.4 POWER SUPPLY

The MMT power supply chassis contains four regulated power supply modules to supply DC voltages of +28V, +15V, -15V and +5V to the RF/IF chassis and the signal processor chassis.

The power supply module specifications allow prime input power to be 105-125 Vac, 50-400 Hz. These power supply modules feature short circuit and overvoltage protection. Full specifications are contained in drawing number X625196.

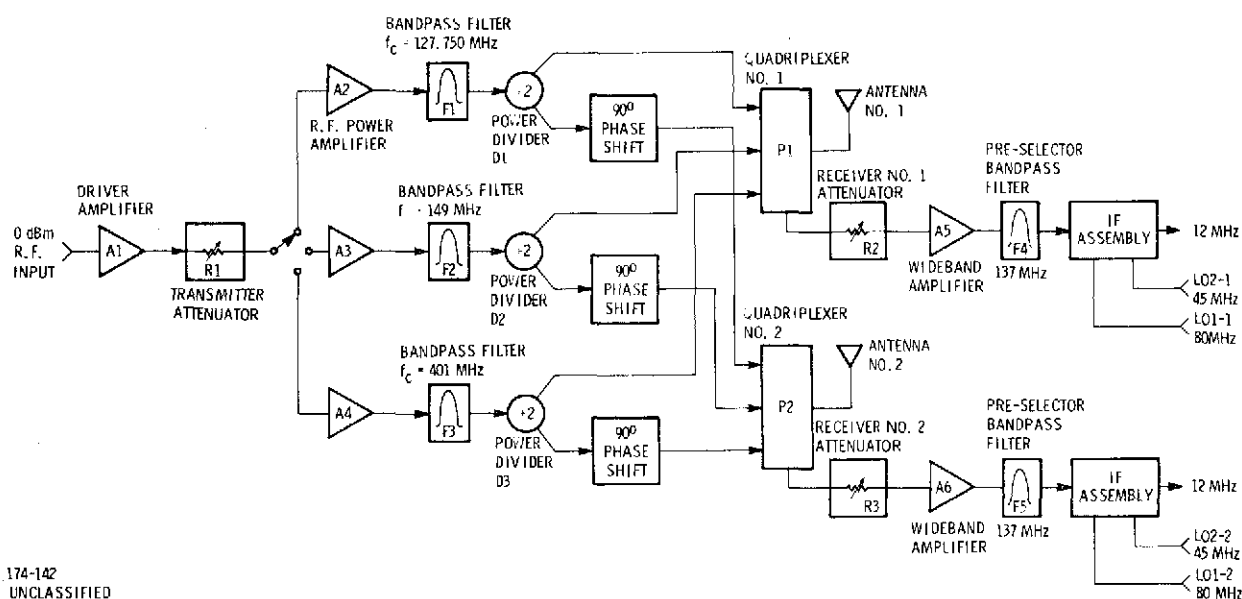
The measured DC power requirements for the MMT are listed below.

+28V	23 watts
+15V	21 watts
-15V	3 watts
+5V	50 watts

3.3 MTAR (GROUND UNIT)

This section describes the Multimode Transmitter and Receiver (MTAR). The MTAR consists of an antenna, RF/IF chassis, signal processor chassis, control box and power supply chassis. The description of the antenna design will be found in paragraph 3.4 of this report.

The MTAR is to perform the same function conceptually as the MMT. The unit is capable of transmitting to and receiving signals from the multimode transponder (MMT) in a number of test configurations in which the MTAR is always ground based. A block diagram of the MTAR RF/IF is shown in figure 3-31. The unit is a combined transmitter and two receivers. The transmitter will transmit one of two VHF frequencies or one UHF frequency.



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Figure 3-31. MTAR RF/IF

3.3.1 RF/IF CHASSIS

The RF/IF chassis contains the high frequency, high power modules that are cabled directly to the antenna connections. There is an antenna port for each of two quadriplexers which isolate transmit power from the receiver inputs. The RF output from the modulator is amplified to the chosen transmit power level in the RF/IF chassis. The RF/IF chassis contains front end amplification, bandpass filtering, and frequency conversion for each of the two diversity receiver channels. Each of the functional elements shown in figure 3-31 is described in the following paragraphs.

3.3.1.1 Driver Amplifier (A1)

The driver amplifier module amplifies the RF signal from the modulator. This module uses a type CA801 broadband RF amplifier. The driver module contains an input resistive network for impedance matching and gain setting. A voltage regulator drops the +28 VDC to the +24 VDC required by the CA801.

3.3.1.2 RF Power Amplifiers (A2, 3 & 4)

The output of the driver amplifier (A1) goes through the transmitter power control attenuator and is switched to drive one of three power amplifiers. Amplifier A2 is connected when a transmit frequency of 127.75 MHz is selected on the control panel. Amplifier A3 is used at 149 MHz and A4 is used at 401 MHz. Amplifiers A2, 3, and 4 are commercial, solid-state linear amplifiers. The total gain of the driver amplifier and power amplifier is approximately 36 dB and all intermodulation products and spurious responses are down at least 30 dB. Using the transmitter alternator the output power is adjustable in 1 dB steps over a 60 dB range. Each power amplifier can deliver 4 watts into a 50 ohm load. The DC power requirement for the power amplifier is +13.8V regulated from +15 VDC.

3.3.1.3 Transmitter Bandpass Filters (F1, 2 & 3)

Each power amplifier is followed by a bandpass filter centered at each of the three transmit frequencies 127.75 MHz, 149.0 MHz and 401.0 MHz. The filters have a 4 MHz, 3 dB bandwidth and an 18 MHz, 45 dB bandwidth. The combination of bandpass filters and quadriplexer provide 110 dB of transmit/receive isolation. The filter characteristics are specified in drawing X625267.

3.3.1.4 Quadriplexers (P1 and P2)

The outputs of the three power dividers are routed into the appropriate ports of the quadriplexers. A quadriplexer permits the use of a common antenna for transmission and reception. Each unit drives one antenna input. Each quadriplexer has a total of five ports, which are (1) 137 MHz, (2) 127.750 MHz, (3) 149 MHz, (4) 401 MHz and (5) the antenna port. The quadriplexers must have adequate isolation since transmitter and receivers are on at the same time. To maintain separation of the transmitter frequency from the receiver frequency, a 110 dB isolation is required between the transmitter band and receiver band. Refer back to table 3-1 for a summary of isolation necessary to obtain separation. The design for the required quadriplexers provides 70 dB of isolation between bands. The other 40 dB is obtained from the bandpass filters.

3.3.1.5 Pre-selector Bandpass Filters (F4, F5)

A bandpass filter is inserted between the wideband amplifier and IF assembly for each diversity receiver channel. The filters are used for additional isolation between transmit and receive frequencies. The receive filter characteristics are specified in drawing X625268.

3.3.1.6 WIDEBAND AMPLIFIERS (A5 & A6)

The 137 MHz receive frequency signal is amplified by a wideband amplifier for each of the two diversity receiver channels. An Avantek UTA-395 wideband amplifier provides 30 dB of gain in each receive channel. For the 137 MHz receive frequency the input to each amplifier is connected to the appropriate quadriplexer port and the output is connected to a bandpass filter.

3.3.1.7 IF Assembly

An intermediate frequency assembly for each receiver amplifies and translates the received signal down to 12.0 MHz. The frequency translation is done in two steps with filtering and amplification at an IF frequency of 57.0 MHz. The input to the IF assembly is connected to a bandpass filter. The local oscillator signals are generated and selected in the Signal Processor Chassis and brought to the RF/IF Chassis via coax cables. In addition to frequency translation and amplification, the IF assembly includes noncoherent AGC circuitry to maintain a maximum 12.0 MHz IF signal level of -24 dBm. The schematic of the IF assembly is drawing X498729.

3.3.2 SIGNAL PROCESSOR CHASSIS

3.3.2.1 Introduction

The MTAR signal processor chassis contains the receiver circuitry from the 12.0 MHz IF down to baseband processing and the transmitter modulator circuitry. The MTAR signal processor chassis is made up of plug-in printed circuit boards. The following is a list of board nomenclature and the quantities used in the MTAR:

Assembly Dwg. No.	PC Board Nomenclature	Quantity	MTAR Location	
X918051	Code & Data Clock Synth.	2	2B06	2B08
X918052	Coder	1	2B07	
X918054	Controller No. 1	1	3B04	
X918047	Controller No. 2	1	3B03	
X918094	MTAR Local Reference/Correlator	2	1B09	3B09
X918058	Baseband Conditioner	2	1B08	3B08
X918059	Carrier Track	2	1B07	3B07
X918060	Code Track	1	2B09	
X918066	PDM Voice	1	1B02	
X918070	TX Data Processor	1	1B03	
X918063	Data Recovery	1	1B04	
X918064	Doppler Input	1	3B05	
X918065	Doppler Arithmetic	1	2B04	
X918090	Doppler Control	1	2B05	
X918092	Doppler Output	1	1B05	
X918067	MMT/MTAR Synth. No. 1	1	2B01	
X918077	MTAR Synth. No. 2	1	2B02	
X918078	MTAR Synth No. 3	2	1B06	3B06
X918071	MMT/MTAR Modulator	1	2B03	
X918093	RF Switch	1	3B02	
X918095	MTAR Oscillator	1	3B01	

3.3.2.2 Controller Board

The MTAR controller board: 1) searches the receiver coder to obtain correlation; 2) interrupts the data stream to send a 31-bit Legendre sequence indicating to the MMT that the MTAR receiver is in sync; and 3) detects the 7-bit Barker sequence transmitted by the MMT and switches to selected data and chip rates from the forced value.

A 31-bit sequence is used to tell the MMT that the MTAR receiver is in sync because the probability that the random data being transmitted by the MTAR before its receiver is in sync will duplicate the sequence is only one 3×10^4 . A 7-bit Barker sequence is sent back from the MMT to initiate the switch to final data and chip rates because no data will be transmitted by the MMT until after this switch has taken place and therefore a long sequence is not required. The 7-bit sequence serves only to eliminate possible false switches due to impulse-type noise interference.

3.3.2.3 MTAR Frequency Synthesizer

The MTAR frequency synthesizer consists of three boards. Boards 1 and 2 are used to generate the fixed frequencies for the transmitter portion of the MTAR. Two each of Board No. 3 are used to generate corrected frequencies for the two receivers of the MTAR. The outputs of the MTAR boards 1, 2 and 3 are specified in table 3-3.

Referring to the block diagram (figure 3-32) of the MTAR, the synthesis of each MTAR output of MTAR board 1 is discussed.

a. 5-MHz Reference Output

The output of the 5-MHz reference oscillator is buffered (EF) on the MTAR board 1 and is presented as a 5-MHz output.

b. 60 MHz (TX-LO) Output

The 60-MHz outputs are basically generated in two steps: first, the 5 MHz is multiplied times 4 to 20 MHz; second the 20 MHz is multiplied times 3 to 60 MHz. The multiplication of the 5 MHz to 20 MHz is done by shaping the 5 MHz into a TTL rectangular pulse (PG-1) of proper duration. The spectrum of a rectangular pulse train is composed of the superimposition of a fundamental cosine wave and its harmonics. The amplitude and phases of the harmonics follow a function of the form:

$$Y = (\sin X) / X$$

where $X = \sin (wt / 2)$ and

$T =$ pulse width

Table 3-3. Specification of MTAR Frequency Synthesizer Outputs

	FREQUENCY IN MHz	POWER LEVEL IN dBm	MIN. ISOLATION From SPURS in dB	USE
MMT/MTAR #1	5.0	0 ±1 dB	>30	Reference
	60.0	+4.0 ±1 dB	>40	TL02C
	60.0	0 ±1 dB	>30	TL02R
MTAR #2	67.75	0 ±1 dB	>40	TL01
	81.25	+4 ±1 dB	>40	TL02B
	333.25	+5 ±1 dB	>40	TL02A
MTAR #3	5.0	TTL Squarewave	N/A	L04-1/2
	10.75	+5 ±1 dB	>40	L03-1/2
	80.0	0 ±1 dB	>30	L01RR-1/2
	80.0	+4 ±1 dB	>50	L01-1/2
	45.0	+5 ±1 dB	>45	L02-1/2

Through imperical analysis using TTL logic as a rectangular pulse generator, it has been found that the pulse width (TP) should be about one half the period of the desired frequency - in this case:

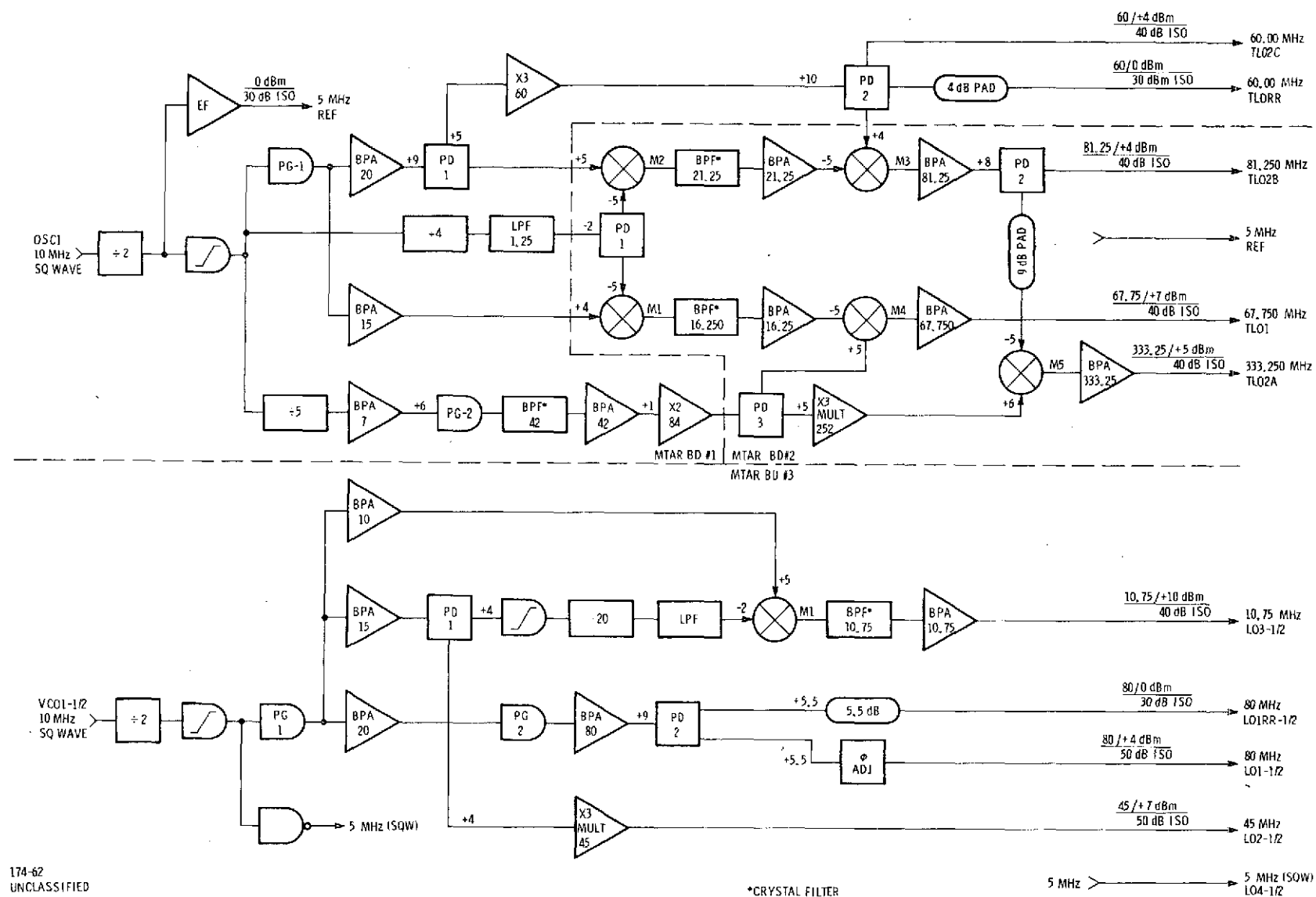
$$TP = \frac{1}{2 f_d} \quad (1)$$

$$\text{where } f_d = 20 \text{ MHz (4 x 5 MHz)} \quad (2)$$

$$\text{then } TP = \frac{1}{2 (2 \times 10^7)} \quad (3)$$

$$TP = 25 \text{ nsec} \quad (4)$$

This places the desired harmonic (20 MHz) in the middle of the first lobe of the sin X/X envelope approximately 3 dB below the fundamental (5 MHz) at the output of PG-1. Now that the desired frequency (20 MHz) has been generated what remains to be done is to filter the 20 MHz from the adjacent harmonics and amplify. This last procedure is implemented with a double-tuned amplifier (BPA-20). The next step, is to multiply the 20 MHz to the desired 60 MHz output frequency. This multiplication is accomplished by driving a class "C" amplifier (X3 - 60) with 20 MHz and tuning the output to the third harmonic or 60 MHz.



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Figure 3-32. MTAR Frequency Synthesizer - Block Diagram

c. 81.25-MHz Output (TL02/3)

The 81.25-MHz output is generated in two basic "mix and amplify" steps. The first mix and amplify step is to generate 21.25 MHz from 20 MHz and 1.25 MHz. The mixer M2 inputs a 20-MHz signal and a 1.25-MHz signal; it outputs the sum and difference of the inputs. Since only the sum (21.25) is desired it is necessary to filter (BPF - 21.25) and amplify (BPA - 21.25) to obtain the desired 21.25-MHz signal. The second step is to mix 21.25 MHz and 60 MHz (provided by MTAR board 1) in M3 and extract only the sum (81.25 MHz). The BPA - 81.25 selects the desired sum from M3 and amplifies the 81.25 MHz to the desired level of +8 dBm. The 81.25 MHz is now applied to the power divider (PD - 4). One of the divided outputs is used as TL02B; the other is employed in the synthesis of 333.25 MHz on MTAR board 2.

d. 67.75-MHz Output (TL01)

The 67.75-MHz output is synthesized in two basic "mix and amplify" steps. The first step is to generate 16.25 MHz from the sum of 5 MHz and 1.25 MHz. The mixer M1 inputs a 15 MHz signal and a 1.25 MHz signal; it outputs the sum and difference of the inputs. Since the sum (16.25) is wanted and nothing else, it is necessary to filter (BAF - 16.250) and amplify (BPA - 16.25) in order to obtain the desired output. The second step is to mix 16.25 with 84 MHz in M4 and extract only the sum of 67.75 MHz. The BPA - 67.750 selects the desired sum from M3 and amplifies the 67.750 to the desired level of 0 dBm.

e. 333.25-MHz Output (TL02A)

The 333.25-MHz output is generated in two basic steps. The first step multiplies the 84-MHz signal from PD3 times 3 to 252 MHz (X3 mult. 252). The second step is to mix and amplify where the sum of 252 MHz and 81.25 MHz is extracted from M5 and amplified by BPA - 333.25 to become the desired output of 333.25 MHz at +5 dBm.

f. 10.75 MHz Output (L03-1/2)

The 15 MHz supplied by BPA - 15 is divided by a factor of 20 to produce a 750 kHz TTL logic output. This output is low-pass filtered to remove all harmonics and is applied to one port of M1. The other port of M1 has 10 MHz applied to it. The output of M1 (sum of 10 MHz + 750 kHz) is filtered and amplified to provide a 10.75-MHz output signal.

g. 80-MHz Outputs (L01RR & L01-1/2)

The 80-MHz outputs are obtained in one basic step. The 20 MHz, supplied by BPA-20, is applied to rectangular pulse generator PG-2 which will generate the fourth harmonic of 20 or 80 MHz. This 80 MHz is now filtered from the adjacent harmonics and amplified by BPA-80. The output of BPA-80 is power split by PD-2 to provide the two 80-MHz outputs needed.

h. 45-MHz Output (L02-1/2)

The 45-MHz output is generated in one basic step. The 15 MHz, supplied by BPA-15, is applied to a times-three tripler which multiplies the 15 MHz to 45 MHz; this now becomes the 45 MHz output (INJ-2).

i. 5 MHz (L04-1/2)

The 5-MHz output is simply a hard-limited divided-by-two version (TTL Logic) of the 10-MHz reference (VCO).

3.3.2.4 MTAR Modulator Board

The MMT/MTAR modulator board is used in both MMT and MTAR. The configuration is changed by moving two RF cable connectors located on the board. Figure 3-33 is a block diagram of the MTAR configuration. The transmit on/off control comes from the controller. The output of the modulator board drives the power amplifier located in the RT chassis. Two operating modes are used:

a. PN Mode

The data to be transmitted is first modulo-2 added to a PN code. The resulting signal then balance-modulates a 67.75-MHz carrier to generate a PSK, spread spectrum signal for transmission. The 67.75 MHz spread spectrum signal is then mixed with one of three transmit LO inputs, amplified and filtered to generate the selected transmit frequency (127.75 MHz, 149.0 MHz or 401.0 MHz).

b. Conventional PSK Mode

The data to be transmitted balance modulates the 67.75 MHz carrier directly instead of being modulo-2 added to the PN code. The 67.75 MHz signal is then mixed with the selected transmit LO to generate the transmitter drive signal.

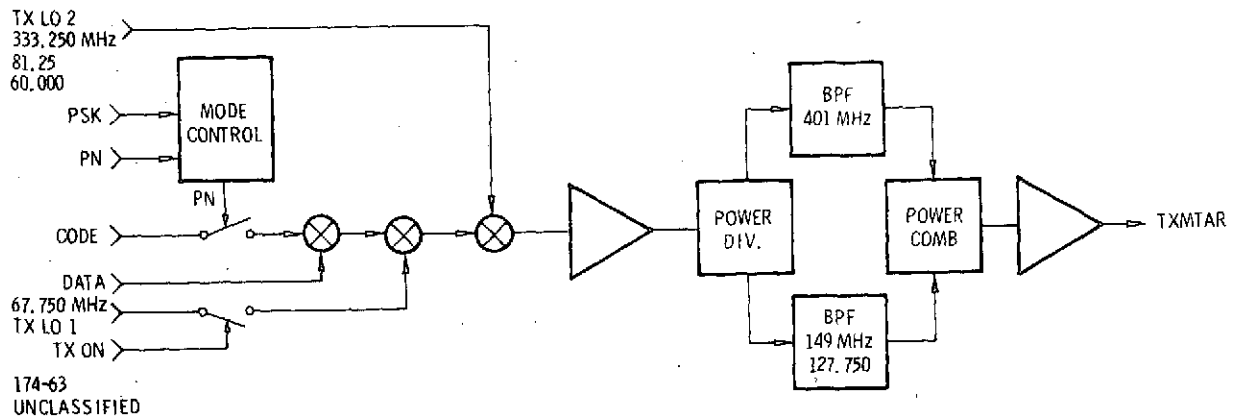


Figure 3-33. Block Diagram, MTAR Modulator Board

3.3.2.5 Code and Data-Clock Synthesizer Board

The code and data-clock synthesizer board provides clocks to the coder, the receive data recovery, and the transmit data processor boards. It also supplies a 4 kHz clock to the controller boards. The clocks to the coder board are at the actual chip rate while the clock to the TX data processor is four times the front panel selected data rate and the clock to the receive conditioner board is eight times the received data rate. Referring back to figure 3-16, the synthesis of the data rate clocks and the fixed 4 kHz signal from the 10.24 MHz VCO/XTAL oscillator. Figure 3-17 is a block diagram of the coder clock synthesis. There are three synthesizer boards in the system. By adding some extra circuitry to the design it was usable in all three different applications.

Starting in the MTAR, one synthesizer board is driven by a crystal oscillator at 10.25 MHz. This board provides a clock to the forward link coder (TX) and the TX data processor. In this application, the step IPM pulse line to the $\div 4$ IPM is left open so that it acts like a simple countdown and the actual code rate is selected by a front panel switch which determines whether the $\div 3$ circuit is included in the countdown chain. Since no data encoding is used in the forward link the 4 times data rate clock is simply divided by four on the TX processor board to provide a clock to the data source. In figure 3-16 the combined divide 16 and divide 128 counters produce an output pulse every 2048 cycles of the 10.24 MHz crystal oscillator. In figure 3-17 this pulse is used to drop one cycle of the 10.24 MHz to the coder clock countdown chain. This process lengthens the code repetition by slipping the coder phase $1/25$ of a bit or $1/75$ of a bit every time it happens. Since the step occurs 25 or 75 time every coder cycle it acts as if it had a period 2048 bits long instead of the actual 2047 bits. This lengthening of the code repetition synchronizes it with the data clock

edges. By so doing it is possible to use a master reset pulse derived from the coder to establish timing for the data clock edges. This eliminates the requirement for a data clock acquisition loop in PN mode. It also phases the doppler resolver. This master reset pulse is brought back from the coder and used to phase the data clock countdown chain on the synthesizer board and on the transmit data processor.

In the MTAR the third synthesizer board is driven by a VCO just as in the MMT. This board performs the same receive function as the MMT synthesizer board. That is, it supplies a clock to the return link receive coder capable of being phase shifted to search for correlation with the received code. It also supplies the appropriate data clock frequency to the return link receive data recovery board.

3.3.3 CONTROL BOX

A remote control box is provided by the MTAR. Front panel switches and indicators are provided to facilitate mode selection for the experiments to be performed.

The following selector switches on the MTAR control box.

- Link Mode - Forward only
Transpond
Return only
- Modulation Mode - PSK
PN

Forward Link

- PN Chip Rate - 34.133 K chip/s
102.4 K chip/s
- Data Rate - 100 bits/s
300 bits/s
1000 bits/s
- Voice
- Frequency - 127.75 MHz
149.0 MHz
401.0 MHz

Return Link

- PN Chip Rate - 34.133 K chip/s
102.4 K chip/s
1024.0 K chip/s

- Data Rate - 0.3 K bits/s
1.0 K bits/s
3.0 K bits/s
10.0 K bits/s
Voice
- Data Encode - ON
OFF

A margin-to-threshold meter scaled in dB is provided for each of the two diversity receivers.

3.3.4 POWER SUPPLY

The MTAR power supply chassis contains four regulated power supply modules to supply DC voltages of +25V, +15V, -15V and +5V to the RF/IF chassis and the signal processor chassis.

The power supply module specifications allow prime input power to be 105-125 VAC, 50-400 Hz. These power supply modules feature short circuit and overvoltage protection. Full specifications are contained in drawing X625196.

The measured DC power requirements for the MTAR are listed below.

+28V	20 watts
+15V	30 watts
-15V	3 watts
+5V	55 watts

3.4 ANTENNA

An antenna was designed and one built (MTAR) by Chu Associates, Incorporated. The antenna was designed for use in the three frequency bands used by the MMT/MTAR equipment as outlined in specification drawing X625198. Figure 3-5 illustrates the MTAR antenna.

Chu associates Incorporated has provided engineering services directed toward the establishment of design specifications for VHF/UHF antenna systems to be used with the Magnavox Research Laboratories Multimode Transponder (MMT) and its associated ground station Multimode Transmitter and Receiver (MTAR) systems. This study was performed under MRL Contract No. XT-707-02 AIM in conformance with the associated Statement of Work.

MMT equipment will ultimately be installed in low-orbiting satellites. For initial test and evaluation purposes, however, it may be installed in an aircraft and operated in conjunction with the associated ground equipment (MTAR). Transmitting and receiving antennas operating in the VHF/UHF band will be required for both the airborne and ground terminals during this evaluation period. Additional testing is required, prior to the airborne evaluation, during which the airborne (MMT) equipment will be located on the ground. The first antenna supplied for the (MMT) equipment will be suitable for use during this ground test period.

3.4.1 GROUND TESTS

3.4.1.1 Multimode Transponder (MMT) Antenna

During the initial test phase, the (MMT) system will be mounted on the ground and will communicate with a ground mounted (MTAR) system. Examination of the general (MMT) antenna requirements indicated three significant areas which would influence the selection of a suitable antenna. First is the relatively wide separation (approximately 3:1) between the VHF and UHF operating frequencies. This wide range tends to preclude use of a single narrow-band antenna to cover all four bands. Many antenna types which exhibit the desired impedance, pattern, and polarization characteristics over narrow frequency ranges would not maintain these characteristics over 3:1 bandwidths. This includes orthogonal dipoles, axial mode helices and fractional turn quadrifilar volutes. Alternate solutions to the wide frequency requirements would be either the use of multiple narrow-band antennas, or a single broad-band antenna having the desired characteristics over the entire band. Various types of log-periodic arrays exhibit these wide-band characteristics, usually at the price of some increase in overall size.

The second consideration is the requirement for full duplex operation - simultaneous transmission and reception - with different polarization requirements for each. Attempting to use a single antenna for both functions would, first of all, require a diplexer capable of isolating a transmitter and receiver potentially separated in frequency by as little as 7 percent. With the common antenna, all space isolation would be eliminated and all of the isolation required for interference-free receiver performance at $f_0 \pm 7$ percent would have to be supplied by the diplexer circuitry. The single antenna approach would also require a radiator which would simultaneously provide a circularly polarized terminal for transmission and multiple polarization

diversity outlets for reception. This could be done with diplexers and phase shifters or by using separate transmitting and receiving antennas, each inherently providing the desired polarization.

The third consideration is the desire for "omni-directional" pattern coverage. In the initial tests, with the (MMT) system mounted on the ground and communicating with a fixed ground based (MTAR), it is felt that suitable pattern coverage would be obtained using one or more unidirectional antennas directed toward the (MTAR). For this point-to-point link radiation in directions other than the (MTAR) would serve no useful purpose. The directional antenna approach would provide additional system gain and would minimize spurious radiation from backlobe reflections.

Reviewing the above considerations, it appears that the simplest approach for the ground based (MMT) antenna system is the use of two antennas, one used exclusively for receiving and the other for transmitting. Each should be unidirectional and oriented to provide maximum radiation along the horizon in the direction of the (MTAR) terminal. The receiving antenna should operate broadband at any of the receiving frequencies, from 126-402 MHz, and have multiple output terminals for selection of the desired polarization. The transmitting antenna requires only a single input terminal providing circular polarization.

For simplicity and economy of design, it is desirable to utilize two identical antenna structures which are capable of providing both the receiving and transmitting characteristics. This can be done with a trapezoidal log-periodic array. The basic array, as shown in figure 3-5 consists of two periodic half-structures oriented at an angle with respect to each other. These two half-structures form a balanced antenna which, when fed against each other from their vertex, radiate a unidirectional beam directed along the apex in the positive Y direction. This radiation is linearly polarized in the plane of the radiating elements. By placing a second pair of half-structures at right angles to the first, sharing a common apex, a second unidirectional linearly polarized beam can be obtained. By feeding each pair separately from coaxial inputs at the rear of the array, two independent, orthogonal, linearly polarized beams can be obtained for polarization diversity. Circular polarization can also be obtained from the same array by combining the two linear pairs with a 90-degree phase shift between them. This can be done inherently by scaling the physical size of one pair of structures to effect a constant 90-degree shift with respect to the other. It can also be done externally, using two in-phase antenna pairs combined through a broadband

quadrature hybrid. The result in either case is a unidirectional, circularly polarized beam.

The radiation characteristics of the array can be controlled by proper selection of the design parameters. For this application, it is desirable to have E and H plane beamwidths which are approximately equal. An array with such beamwidths, designed to operate over the entire 126-402 MHz range, would be pyramidal in shape with a square base of approximately 54 inches on a side and a base-to-apex height of approximately 36 inches. Each linear array would have a 1/2 power beamwidth of about 65 degrees in the E-plane and 70 degrees in the H-plane. The gain of one array would be in the order of 8 DBI with front-to-back ratios of 12-15 dB. The input VSWR on 50 ohms would be less than 2.0:1 at all frequencies.

For receiving it is not known what degree of polarization diversity is desired as two orthogonal linear modes and a circular mode can be obtained. If the two linear modes are sufficient, they are available from the two antenna feed ports without need for the switches or hybrid. Similarly for transmitting, which requires only circular polarization, the two inputs from the antenna would be connected directly to the hybrid.

3.4.1.1.1 Multimode Transmitter and Receiver (MTAR) Antenna

During the ground test phase of this program, the companion (MTAR) equipment can utilize the same type of antenna described above for the (MMT) equipment. Two trapezoidal log-periodic arrays would be mounted side by side and oriented for maximum radiation in the direction of the (MMT) ground site. One antenna would be configured for polarization diversity reception in the 136-138 MHz band. The other would be configured for circularly polarized transmission in the 126-130, 148-150, and 400-402 MHz bands.

Use of identical antenna systems for both the (MMT) and (MTAR) terminal offers the most economical approach and will provide maximum system flexibility.

3.4.1.2 Airborne Tests

During the airborne test phase of this program, the (MMT) terminal will be installed in an aircraft and operated in conjunction with the ground-based (MTAR) equipment. From the standpoint of electrical performance, the same log-periodic array could be utilized. The primary limitation on test flexibility is the pattern

coverage that can be obtained. Because of its inherent directional characteristics, the coverage obtained on the aircraft will not differ greatly from the ground-based condition. As discussed, the E and H plane half-power beamwidths of this array are nearly constant at approximately 65 degrees to 70 degrees. Assuming a nominal gain of 8 dBi for the linear polarized mode, the beamwidth over which the response is above isotropic level is approximately 120 degrees. Beyond this point the response decreases steadily and reaches low levels at angles normal to the axis. This will limit the flight pattern of the aircraft, depending upon where the antenna is mounted on the aircraft and also upon the orientation of the ground antenna.

With the array mounted off the side of the aircraft, normal to the line of flight and angled downward toward the ground, the aircraft could make straight fly-bys some distance away from the ground site, generally observing the 120-degree sector limitation. Maximum signal level would be obtained during this flight pattern by tilting the ground antenna toward the line of flight. Obviously on the return fly-by the aircraft array would be pointed away from the ground site and relatively little response would be obtained.

Greater usable pass time could be obtained by flying circular patterns at a fixed radius from the ground site. During such passes, the ground antenna could be tilted to favor a particular path sector. It could also be mounted vertical for uniform, but reduced, response over the entire circle.

Depending upon the type of aircraft used, it may also be operationally feasible to mount the array near the rear of the fuselage pointing aft and downward. This would permit radial passes, vectored outward from the base site. For optimum response, the base antenna should be tilted toward the direction of flight.

The most severe obstacle to use of the log-periodic arrays for flight tests is one of mechanically adapting them for installation on the aircraft. It will be a major task to ruggedize these arrays and suitably fit two of them to the aircraft environment. Every effort should be made to minimize this task. It would be highly desirable for the airborne terminal to utilize a single antenna array suitable for simultaneous transmitting and receiving use.

It should be noted that the requirement for reception in the 126-130 MHz and 400 MHz bands would require a base width of approximately 50 inches and base-to-apex height of about 34 inches.

A cursory wind load analysis was made for the worst-case condition, with an array mounted on the side of the aircraft, normal to the direction of flight. Using radiating elements of 3/8-inch diameter, dielectrically braced at the edges to the adjoining array, the size of the central support tubes would vary from approximately 1 1/4-inch O.D. with 3/32-inch wall at speeds of 100 knots to 2 1/4-inch O.D. with 3/16-inch wall at 250 knots. At 175 knots (200 mph) tube sizes in the order of 1 3/4-inch O.D. would be required. It is felt that a satisfactory electrical design could be obtained within these physical design parameters.

It is visualized that the most simple means of installing this antenna on the aircraft would be a fixed, base mounted against a side door or bottom cargo hatch. Base mounting should provide maximum support for the antenna and would require minimum aircraft modification. An alternate method would be to support the antenna from the end of a movable boom extending horizontally out from a side door. Axial rotation of the boom would turn the array to point toward the ground during test or swing it upward, if necessary, for clearance while on the ground. The best method will obviously be dependent upon the type of aircraft selected for the tests. It may also be necessary to incorporate means for folding the array for stowage against the side of the aircraft in essentially a two dimensional triangular shape. This, of course, would complicate the mechanical design and should not be done unless necessary under the operating conditions.

3.4.1.3 Design Specification

It is recommended that the coincident orthogonal trapezoidal log-periodic arrays discussed above be utilized for both the (MMT) and (MTAR) terminals. For greatest simplicity and economy both terminals should use the same antenna configuration. The (MMT) antenna system should be designed during the ground test phase to permit direct adaption of the same antenna to the aircraft during subsequent airborne phases of the program.

Each antenna will be identical in electrical performance. Each would consist of identical orthogonal arrays with dual coaxial outputs. These outputs would be in-phase, but would provide orthogonal linear polarization. They would provide circular polarization when externally combined through an external 90-degree phase shifter as part of the terminal equipment.

The (MMT) terminal, at least during the airborne phase, should use a single antenna for the receive and transmit modes. This requires a quadriplexer and phase shifters as part of the terminal equipment. It is recommended that the same configuration be used during the ground phase and also for the (MTAR) terminal, although, if desired, separate receiving and transmitting antennas could be used to eliminate the diplexer requirement.

Each array should have the following electrical characteristics:

Frequency range:	126-402 MHz covering four discrete bands; 126-130, 136-138, 148-150, 400-402 MHz
VSWR:	2.0:1 maximum on 50 ohms in each frequency band
Outputs:	Dual 50 ohm coaxial
Pattern:	Unidirectional with each linear array displaying average half-power beamwidths of: E-plane = 65° H-plane = 70°
Front-to-Back ratio:	15 dB average
Gain:	6 dBi, each linear input

3.5 TEST EQUIPMENT AND INTERFACE

Two MX 270B bit error rate analyzer instruments are included with the MMT and MTAR equipment. The MX 270B is used to measure system performance by measuring digital data error rates.

This section describes the theory of operation of the MX 270B. A general block diagram level is presented first followed by a more detailed description of each of the main MX 270B functions. These functions are further explained depending upon the circuit complexity.

3.5.1 THEORY OF OPERATION

A simplified block diagram of the MX 270B is shown in figure 3-34. There are four basic sections in the MX 270B: a) transmitter, b) receiver, c) counter, and d) power supply. During operation, a clock pulse received from an external (or internal) source generates a data pattern selected by the front-panel controls. The modem under test demodulates the data pattern and supplies the demodulated data

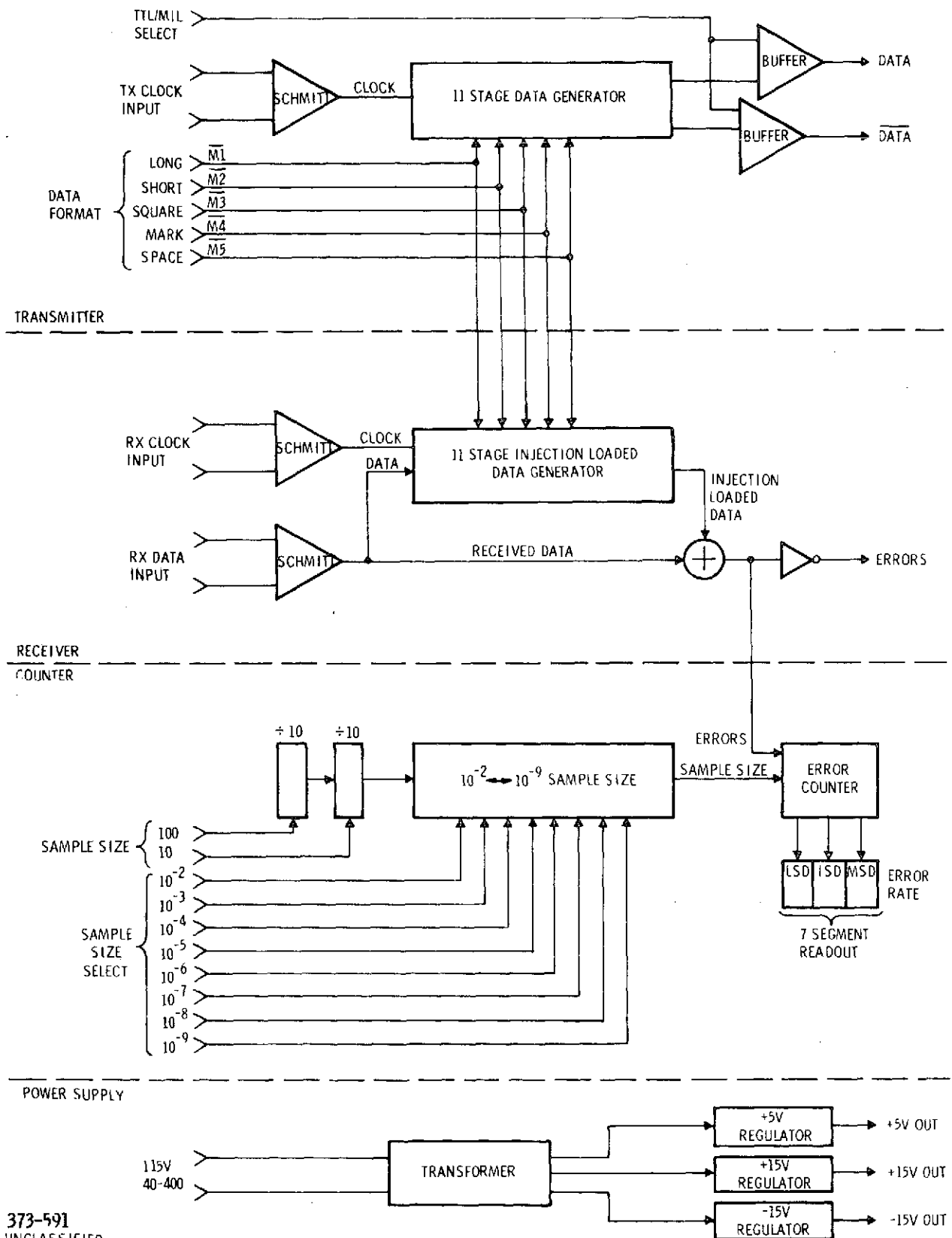


Figure 3-34. MX 270B Functional Block Diagram

pattern along with the data clock back into the receiver section of the MX 270B. The MX 270B then injection loads a similar data pattern generator and compares the injection loaded pattern with the modem demodulated data pattern in a bit-by-bit comparison to generate an error pattern. This error pattern is then counted over a selected number of bits determined by the $X10^{-}$ front panel control and the SAMPLE SIZE control. The selected sample size error rate is then displayed on the ERROR RATE indicator.

3.5.2 MTAR/MMT MONITOR SIGNALS

Table 3-4 presents a list of the monitor signals available from either the MTAR or MMT equipment.

Table 3-4. MTAR/MMT Monitor Signals List

J1	SYMBOL	SIGNAL DESCRIPTION
A	MP5V	+ 5 Volt Power Supply Access
B	MP15V	+15 Volt Power Supply Access
C	M-15V	-15 Volt Power Supply Access
D	MP28V	+28 Volt Power Supply Access
E	MRT28V	+28 Volt Return
F	GDPLATE	Chassis Ground
G	AUDIN1	Transmit Audio Input (Ground) } Configured for Transmit Audio Input (Signal) } Carbon Mike (Impedance: 600 Ω , Input: 80 to 1400 mV rms)
H	AUDIN2	
J	--	
K	AUDHI	Received Audio, 6.7 VRMS
L	AUDLO1	Received Audio Output } Balanced Pair, Received Audio Output } 600 Ω , 3 VRMS
M	AUDLO2	
N	DATARX	Received Data TTL
P	CLKREC	Received Data Clock TTL
R	TLMTX*	Data to XMTR TTL
S	1XDTCLK*	Data Clock to XMTR TTL
T	AGNC-1	Channel -1 Noncoherent AGC (-0.7 to +15V)
U	AGNC-2	Channel -2 Noncoherent AGC (-0.7 to +15V)
V	AGF-1	Channel -1 Coherent AGC (-0.7 to +15V)
W	AGF-2	Channel -2 Coherent AGC (-0.7 to +15V)
X	AGCMB	Common Coherent AGC (-0.7 to +15V)
Y	THRESH-1	Channel -1 Margin to Threshold (0 to +5V)
Z	THRESH-2	Channel -2 Margin to Threshold (0 to +5V)
a	SEL-1	Channel -1 Selected } Diversity RCVR Channel -2 Selected } Selection TTL
b	SEL-2	
c	READY	Two-Way Link Established TTL
d	TXON	Transmitter ON TTL
e		
f		
g		
h		
j		

*CMDTX and 1XDTCLK for MTAR Equipment.

3.5.3 EXTERNAL INTERFACE SIGNAL SPECIFICATIONS

Antenna Input

Impedence	50 Ω Resistive
Level	-90 to -150 dBm
Connector	Type N
Frequency	127,750 to 401 MHz

Prime Power

Voltage	110-120 V, AC, 50-400 Hz
Power	300 Watts Max.
Connector	STD. AC Receptacle

MX-270 Data Error Pulses

Pulse Level	TTL
Pulse Width	1/Data Rate
Connector	BNC. Coaxial
Pulse Rate	0 to 100 PPS.

3.5.4 RANGE AND RANGE RATE SIGNAL SPECIFICATIONS

Start

Connector	TNC Coaxial
Waveform	Pulse
Load	50 Ω Resistive
Level	0.1 Volt True 0 Volt False
Width	1 mS for 1024.0 KCS Code 10 mS for 102.4 KCS Code 30 mS for 34.1 KCS Code
Rate	60 mS for FWD Link 34 KCS RTN Link 34 KCS 40 mS for FWD Link 102.4 KCS RTN Link 102.4 KCS

120 mS for FWD Link 102.4 KCS

RTN Link 34 KCS

Stop

(Same as above)

Range Rate (RR-1)

Channel	#1
Level	0 dBm \pm 1 dB
Load	50 Ω Resistive
Frequency	80 MHz Nominal
Waveform	Sinewave, Continuous
Connector	TNC on Sig. Proc. Front Panel

Range Rate (RR-2)

Channel	#2
Level	0 dBm \pm 1 dB
Load	50 Ω Resistive
Frequency	80 MHz Nominal
Waveform	Sinewave, Continuous
Connector	TNC on Sig. Proc. Front Panel

Reference

Frequency	5 MHz
Level	0 dBm \pm 1 dB
Load	50 Ω Resistive
Waveform	Sinewave
Connector	TNC on Sig. Proc. Front Panel

SECTION IV

MECHANICAL DESCRIPTION

This section provides a detailed mechanical description of each of the major assemblies which are included in the Multimode Transponder equipment group. Each of the unique chassis are shown pictorially and the dimensions, weight and construction technique for each major unit is illustrated in detail. Finally, the environmental and maintainability philosophy used for the design of the Multimode Transponder equipment is presented.

4.1 MAJOR ASSEMBLIES

The TDRSS Multimode Transponder equipment complement consists of the airborne MMT system and the MTAR ground system. Mechanically, the two systems are nearly identical with the chief differences being panel layouts and/or placement of electronics.

Each system consists of six assemblies: signal processor, receiver-transmitter, control-display panel, power supply, bit error rate analyzer and a signal monitor box. In addition an antenna is supplied with the MTAR equipment. A Multimode Transponder equipment list is shown in table 4-1.

Table 4-1. Multimode Transponder Equipment List

Nomenclature	P/N	S/N
MTAR Control Display Panel	930751	1
MTAR Signal Processor	930770	1
MTAR Receiver-Transmitter	930754	1
MTAR/MMT Power Supply	930753	1
MTAR Antenna	625198	1
MMT Control Display Panel	930752	1
MMT Signal Processor	930771	1
MMT Receiver-Transmitter	930771	1
MTAR/MMT Power Supply	930753	2
MX 270B Bit Error Rate Analyzer	918654	1
MX 270B Bit Error Rate Analyzer	918654	2
MTAR/MMT Signal Monitor Box	631111	1
MTAR/MMT Signal Monitor Box	631111	2

4.2 RECEIVER-TRANSMITTER

The Receiver-Transmitter chassis contains all the RF subassemblies down to the 2nd IF for both diversity receivers and the RF power amplifiers for the transmitter. It houses all switching relays for use in selecting one of four RF frequencies, the bandpass filters for each of these frequencies and the quadriplexers which isolate the received signals from the transmitted signals. The MTAR and MMT Receiver-Transmitter chassis are shown in figure 4-1 and 4-2.

Pertinent mechanical specifications include:

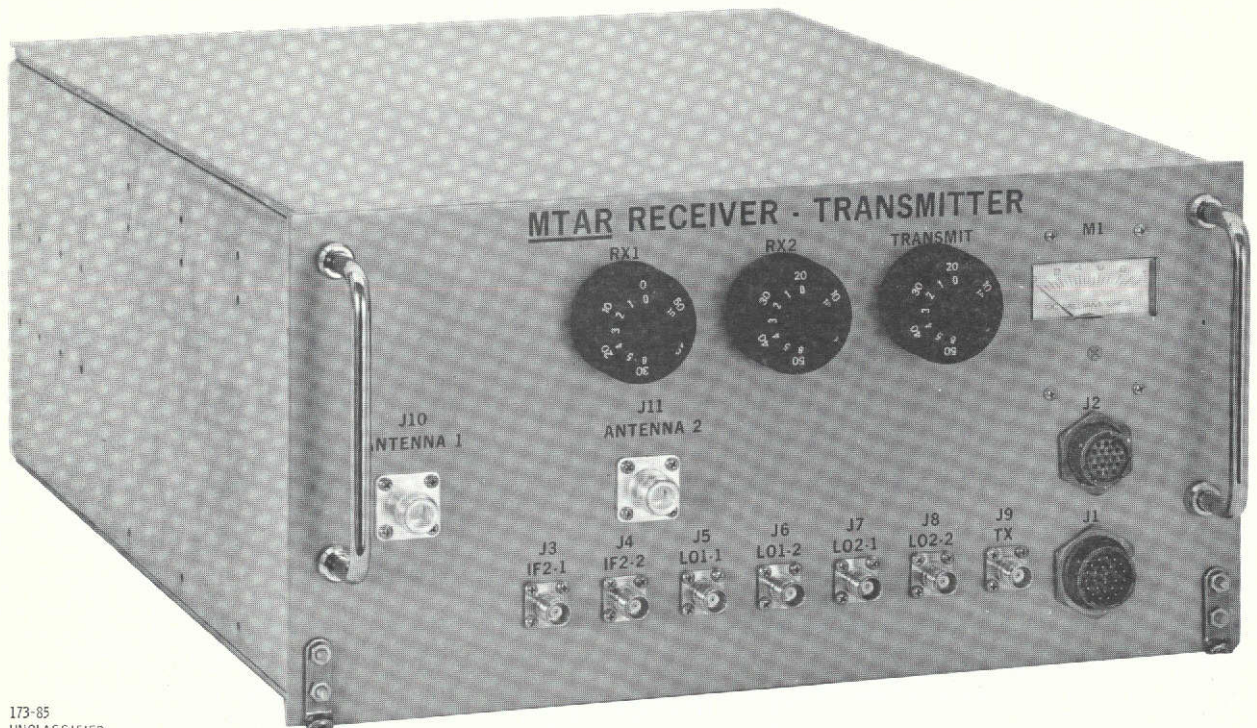
• Size	15.38W x 7.63H x 18.10L
• Cooling	Natural convection
• Weight	MTAR = 38 lbs MMT = 33 lbs
• Construction	Sheet aluminum riveted assembly

Basic construction of the unit is a simple brazed sheet aluminum box. The case is RF sealed by utilization of RF gasketing at the top cover. Since power dissipation is low and cooling is by natural convection, conduction and radiation to the case is adequate. All input-output power and signal connectors as well as the power attenuator(s) are located on the front panel. A standard holddown arrangement is provided for mounting in a MS 91405 type mounting tray. Access to all components is from the top. The cover is provided with 1/4 turn fasteners to speed removal.

The front panel contains two antenna ports for polarization diversity operation. For experimental purposes there are two RF attenuators for adjusting the RF signal level into the two diversity receivers. A third attenuator controls the output level of the transmit signal. A meter monitor is used to verify the presence of an RF transmit signal. TNC connectors interface the first and second L.O.'s and transmitter drive from the Signal Processor and the second IF outputs to the Signal Processor.

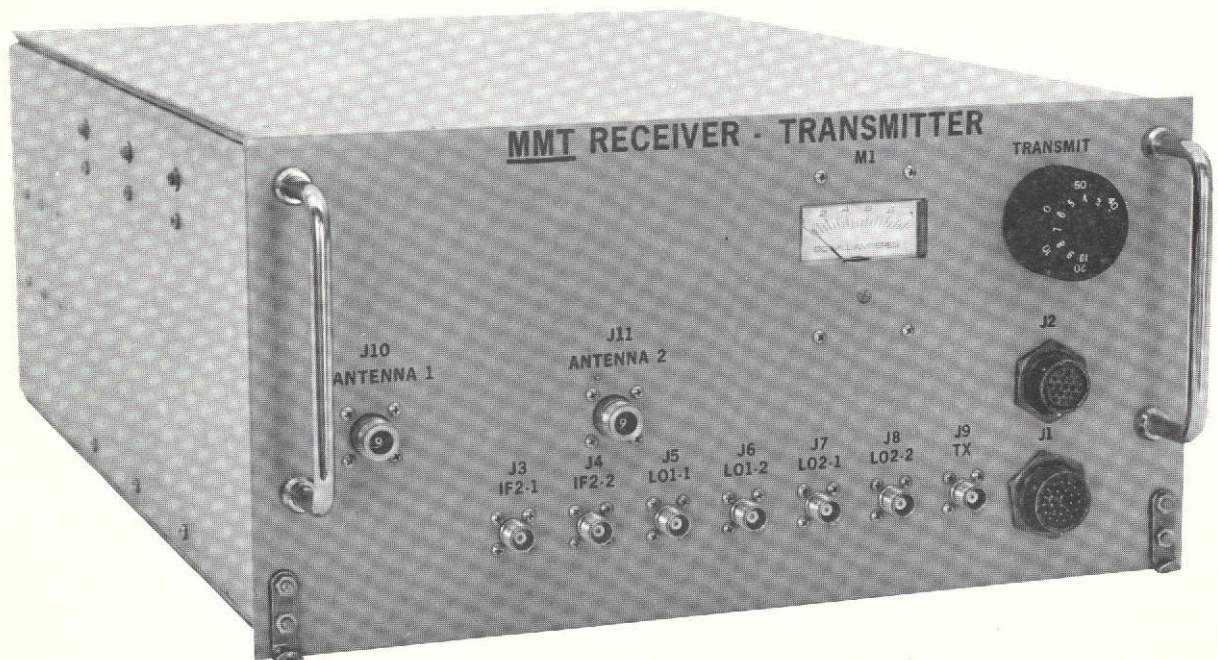
4.3 SIGNAL PROCESSOR

The Signal Processor chassis contains most of the IF subassemblies and all of the baseband processing for both the receive and transmit functions. The MTAR Signal Processor chassis is shown in figure 4-3. The MMT Signal Processor is the same in appearance except for the range rate and range interface.



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Figure 4-1. MTAR Receiver-Transmitter



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Figure 4-2. MMT Receiver-Transmitter

Pertinent mechanical specifications include:

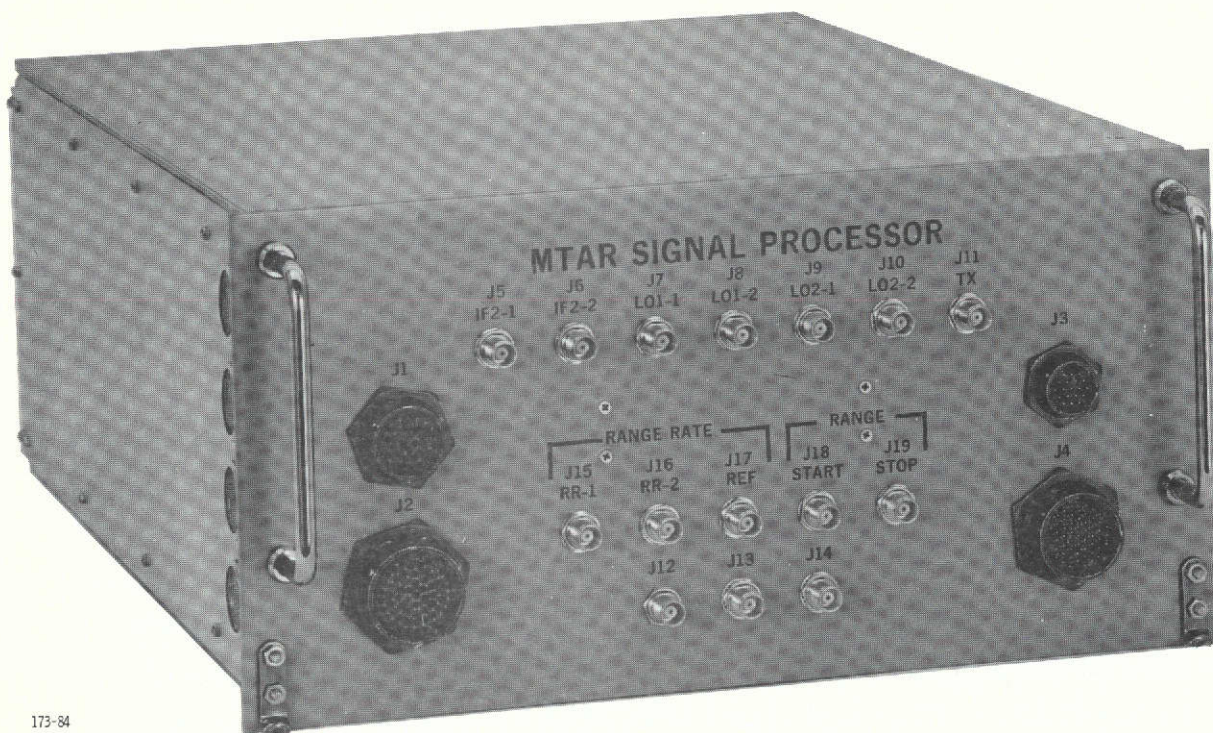
•	Size	15.38W x 7.63H x 18.10L
•	Cooling	Forced air convection
•	Circuit Cards	27
•	Card Size	Nominal 4x6
•	Weight	36 pounds
•	Construction	Sheet aluminum riveted assembly with honeycomb sections between card rows.

The signal processor is a basic 1-1/2 ATR size, 15.38 inches wide x 7.63 inches high x 18.10 inches long. The design is generally in accordance with the requirements of MIL-C-172. Structural and environmental design was based upon installation aboard a transport type aircraft like a C-121G. See figure 4-4 for an illustration of the basic chassis configuration.

Basic construction of the unit is sheet aluminum, with internal honeycomb sections that impart structural strength in addition to the primary task of providing free passage of cooling air and RFI protection between rows of circuit boards. A standard holddown arrangement is provided for mounting in an MS 91405 type mounting tray.

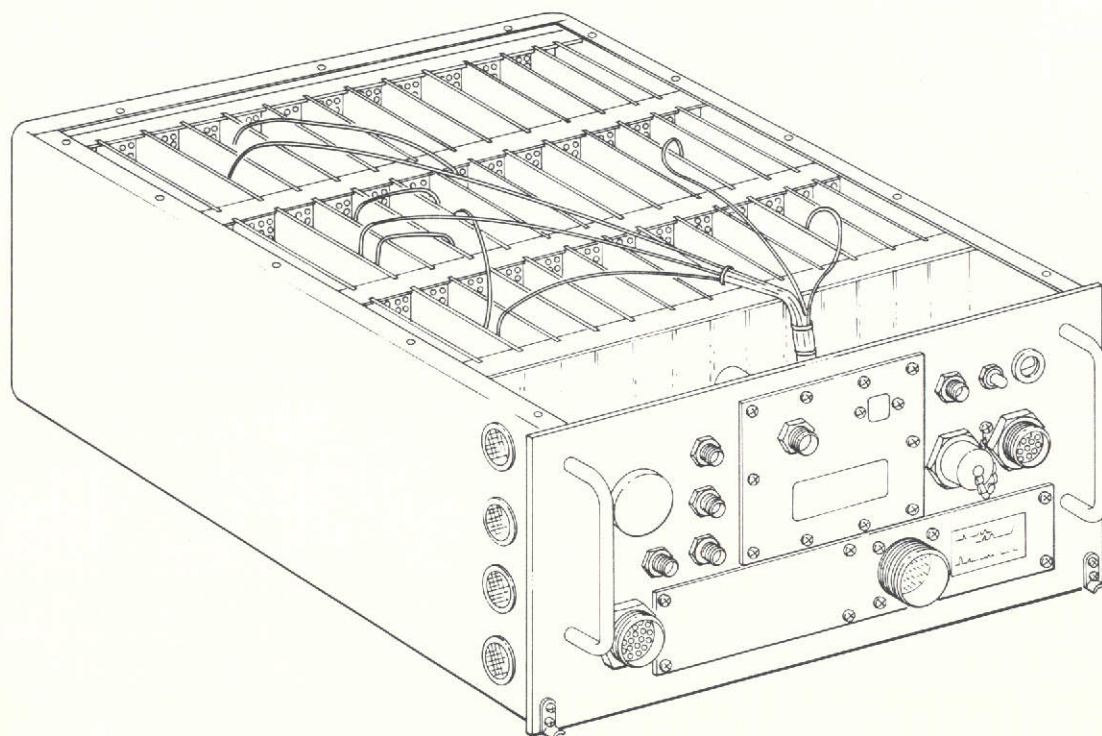
All interface connectors are located on the front panel. Both the top and bottom covers are provided with 1/4 turn fasteners to enhance removal and reduce downtime. Access to test points on the circuit boards and module cans is provided from the top of the unit. All wiring with the exception of some RF module coax interconnects is done from the bottom. Both front and rear panels are detachable to provide easy access during wiring and/or service operations. Basic circuit card layout is divided into functional groupings. As indicated in figure 4-4, the boards are separated into three rows with honeycomb sections between rows providing RF protection. In addition, metallic shields are located between individual boards to provide increased isolation.

The front panel of the Signal Processor contains TNC connectors to provide the L.O.'s and transmitter drive signal to the Receiver-Transmitter and accept the IF output signals from the Receiver-Transmitter. On the MTAR Signal Processor front panel, terminals J₁₅ - J₁₉ are TNC connectors which interface with



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Figure 4-3. MTAR Signal Processor



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Figure 4-4. Basic Signal Processor Chassis Configuration

a Computing Counter for range rate and range measurements. J_{12} - J_{14} are spare TNC connectors. Four hard wire connectors interface with the Power Supply, Control-Display Panel and the Receiver-Transmitter assemblies.

4.3.1 PRINTED CIRCUIT SUBASSEMBLIES

The internal board rack is divided into three sections separated from each other by the honeycomb partitions. Each section is further divided into functional groupings of printed circuit board separated by RF shields. See figures 4-5 and 4-6 for the MTAR and MMT signal processor plan views, indicating card locations. Packaging of the circuit elements makes broad use of microelectronic techniques. The circuit boards, supported in the case by means of metallic card slides, plugged into printed circuit edge connectors located on the connector plate at the bottom of the unit. Circuit boards are keyed to reduce possibility of harmful effects from improper signals when plugged into the wrong slots. In addition all like voltages are assigned the same pin location for all circuit boards and connectors. All circuit boards are 4.00 inches by 6.00 inches with 50 edge contacts for input-output power and signal connections. In addition, each card will have an edge contact at the top which provides 20 test-point connections.

There are basically two types of printed circuit board subassemblies. The first type is a multilayer (5-7 layers) PC card used where the design dictates the use of ground and voltage planes or high density layouts to minimize influence from the surrounding environment. The second type is a 2-layer board in a universal configuration where all the circuits are point-to-point wired. This second technique is cost effective for low quantity fabrication (1-6 pieces), is suitable for most logic circuits and lends itself to easy modification during checkout and system integration. As examples of the two techniques, figure 4-7 shows the PDM voice modulator/demodulator card which is a five layer PC board and figure 4-8 shows the PN coder card which is a point-to-point wired universal PC board.

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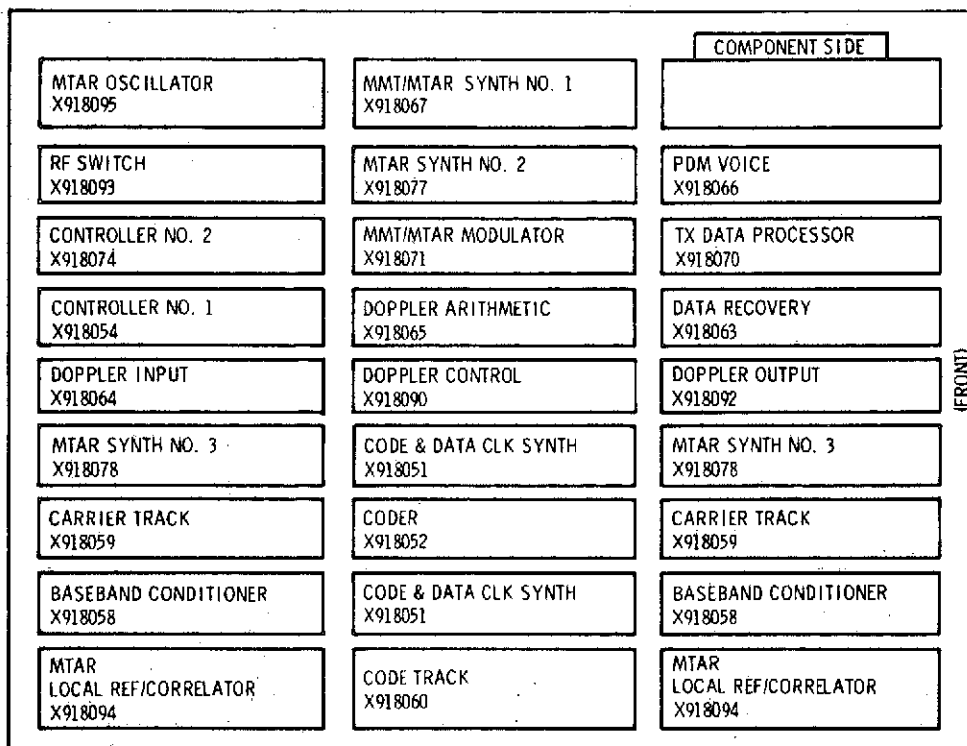


Figure 4-5. MTAR Signal Processor PC Board Placement (Top View)

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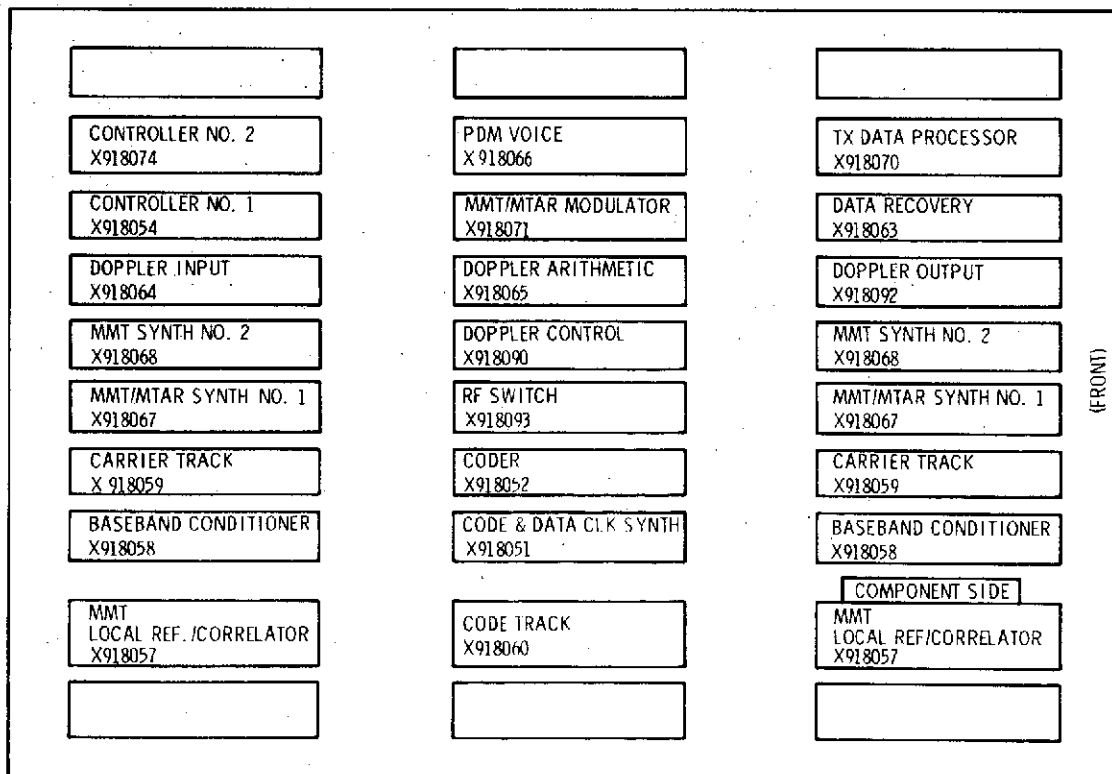
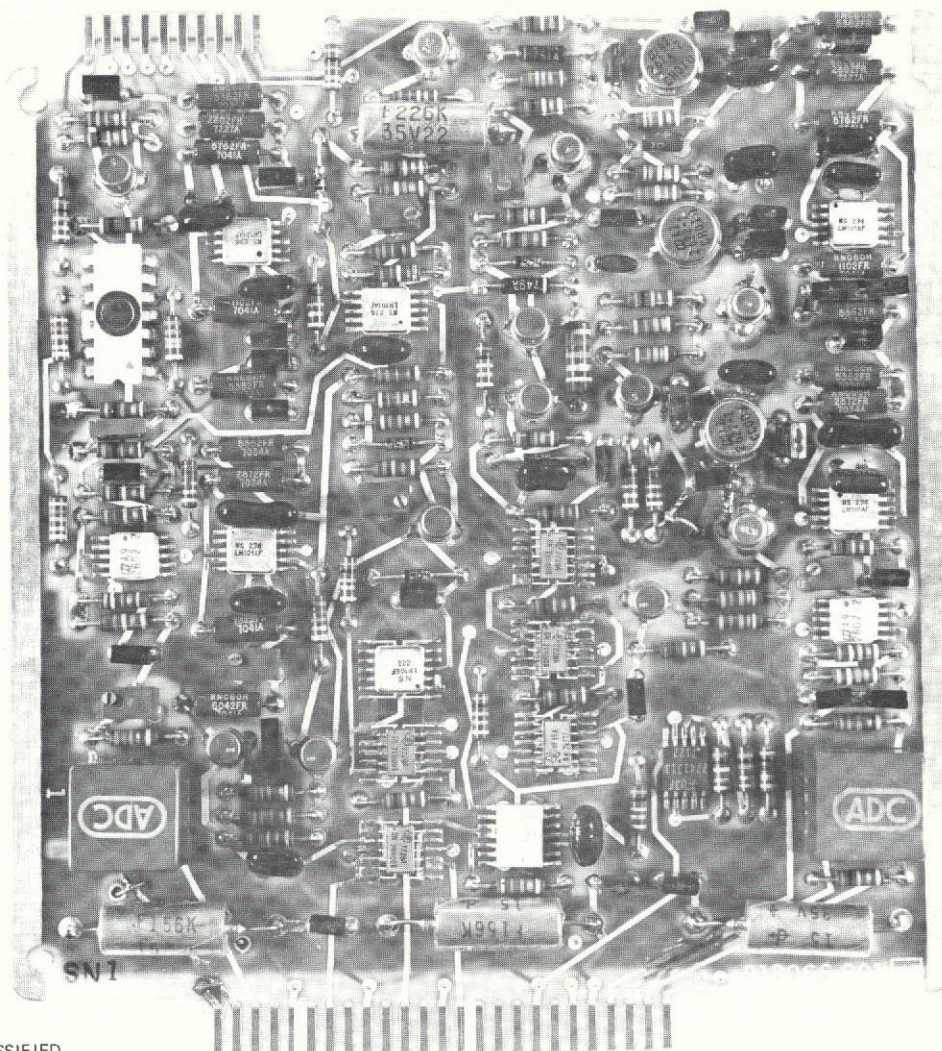


Figure 4-6. MMT Signal Processor PC Board Placement (Top View)

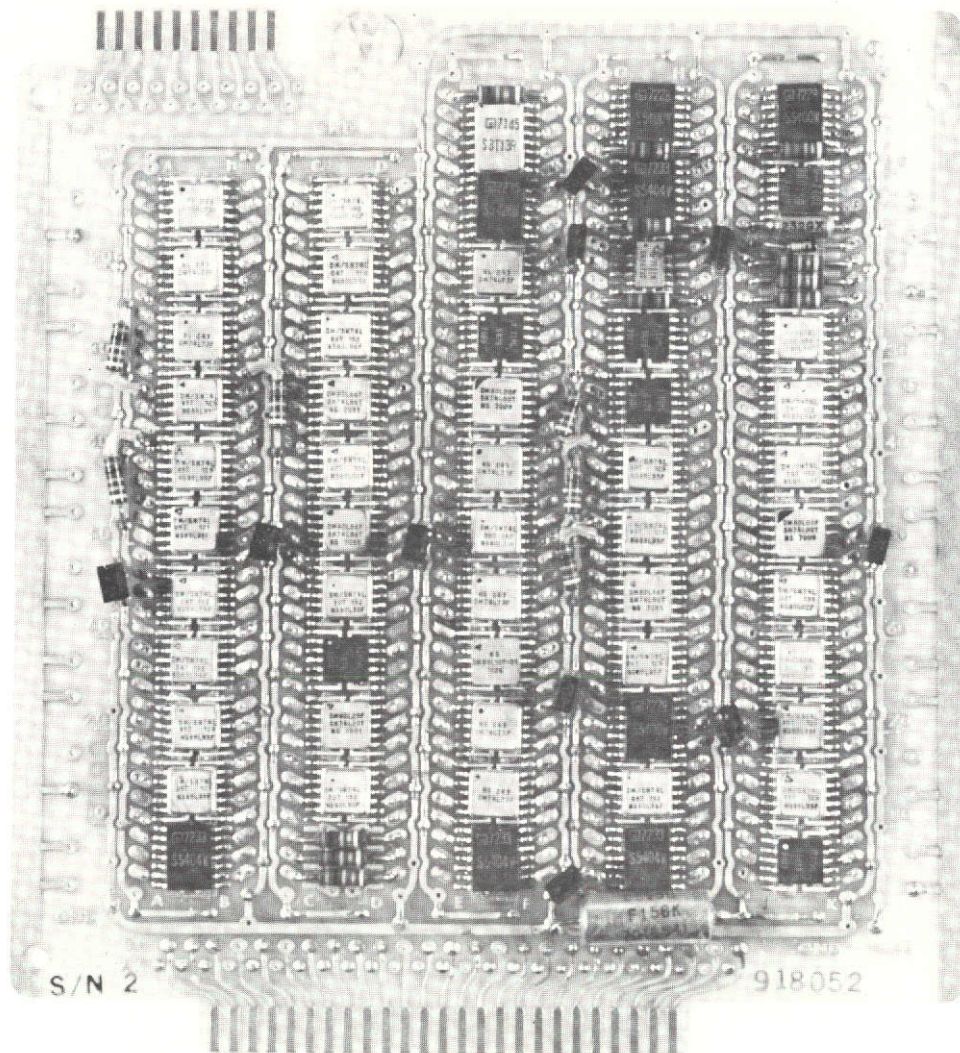


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Figure 4-7. PDM Voice Mod/Demod PC Card

4.4 CONTROL-DISPLAY PANEL

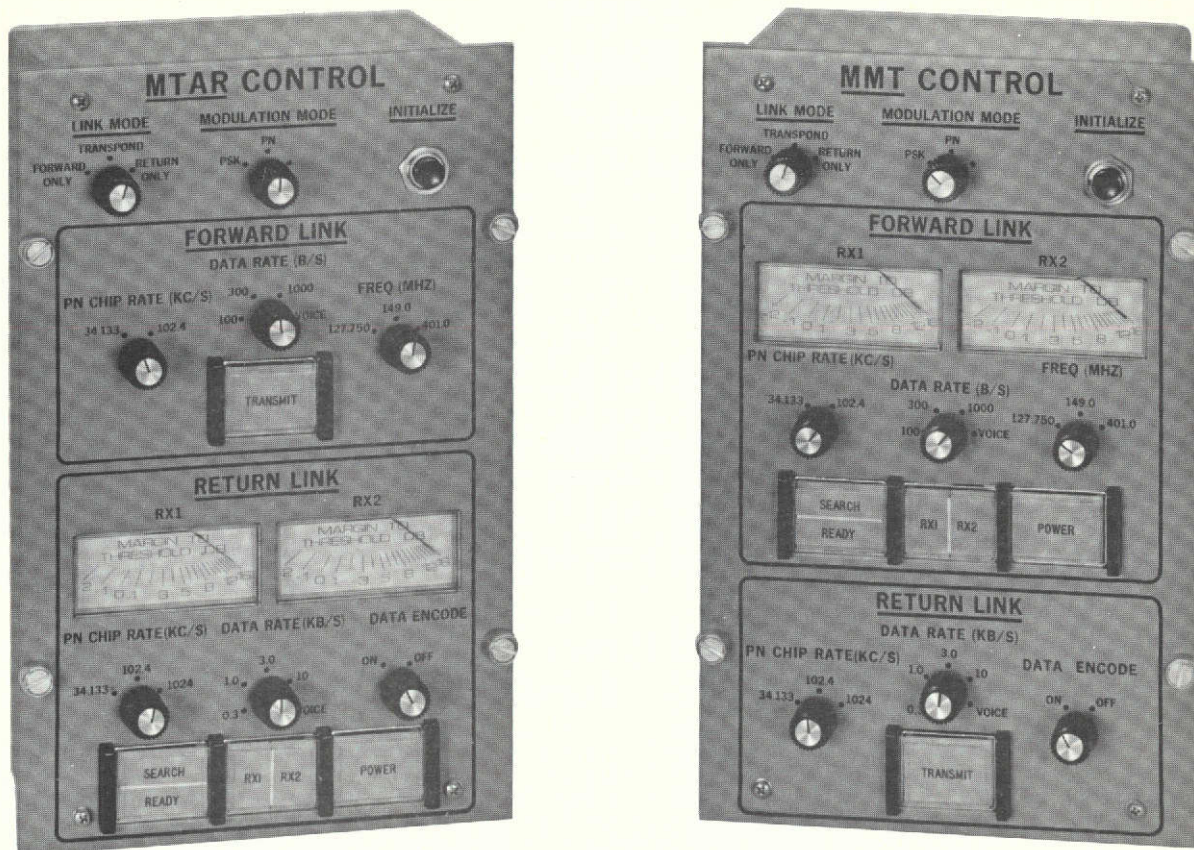
The MTAR and MMT Control Display Panels are shown in figure 4-9. From these units, all modes of operation for the Multimode Transponder equipment are selected. Notice from figure 4-9 that, except for the "Mode" controls, all controls are located within the partitioned areas designated "Forward Link" or "Return Link".



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Figure 4-8. PN Coder PC Card

When either unit is transmitting a red lamp marked "Transmit" illuminates. Prior to acquisition, while each system is searching for a signal to acquire, an orange lamp marked "Search" illuminates. After a terminal has acquired and synchronously switched to the selected mode of operation, the green lamp marked "Ready" illuminates. Meters are provided which indicate the "Margin-to-Threshold" for each receiver. Power is applied to the system by depressing the display window marked "Power". Power is removed from a system when this window is again depressed. As long as power is applied, this window remains illuminated.



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Figure 4-9. MTAR and MMT Control/Display Panels

Pertinent mechanical specifications include:

- Size 5.75W x 9.00H x 3.00L
- Cooling Natural convection
- Weight 3 pounds
- Construction Sheet aluminum riveted assembly

The control unit chassis is 5.75 inches wide x 9.00 inches high x 3.00 inches deep. Structural and environmental design is based upon installation aboard a transport type aircraft. Basic construction is sheet aluminum. Total weight is 4 pounds. All controls and displays are located on the front panel. Wiring is behind the panel. A dust cover protects the rear portions of all components. Panel size and fastener arrangement is generally in accordance with MS 25212.

4.5

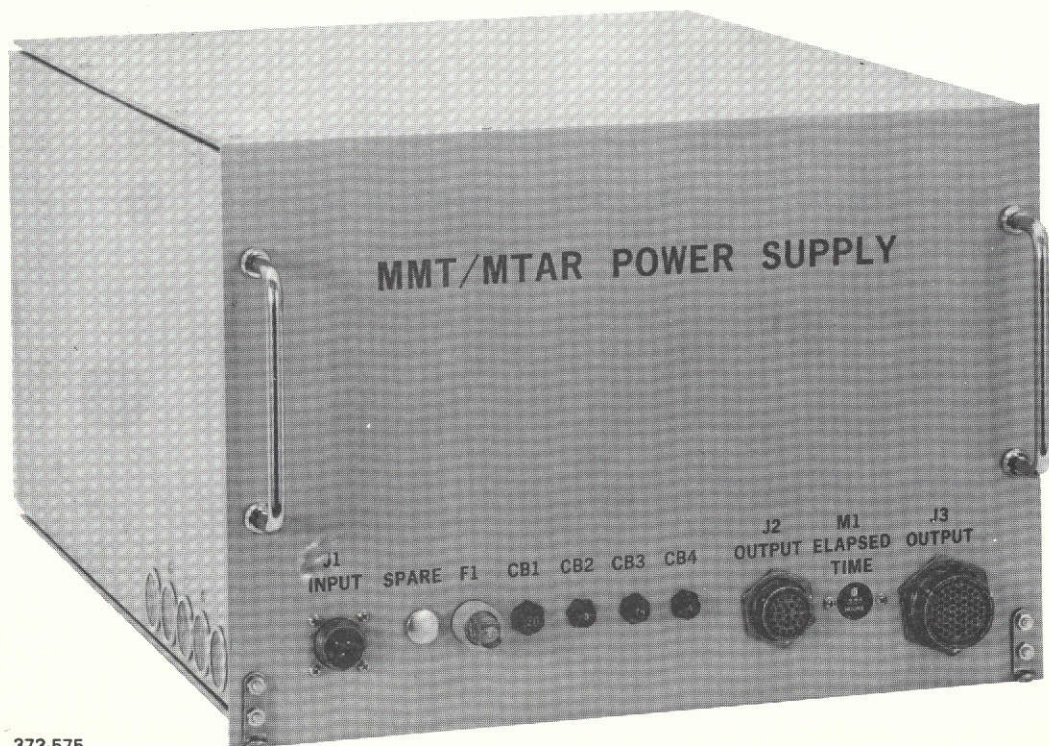
POWER SUPPLY

Both the MMT and MTAR equipments use a power supply which is shown in figure 4-10. Each power supply chassis contains individual power supply modules for each supply potential. The prime power requirements are as follows:

Voltage:	115 VAC
Current:	2 amps, max.
Frequency:	60-400 Hz
Phases:	Single phase

The power supply output potentials are as follows:

- +28 VDC
- +15 VDC
- 15 VDC
- + 5 VDC



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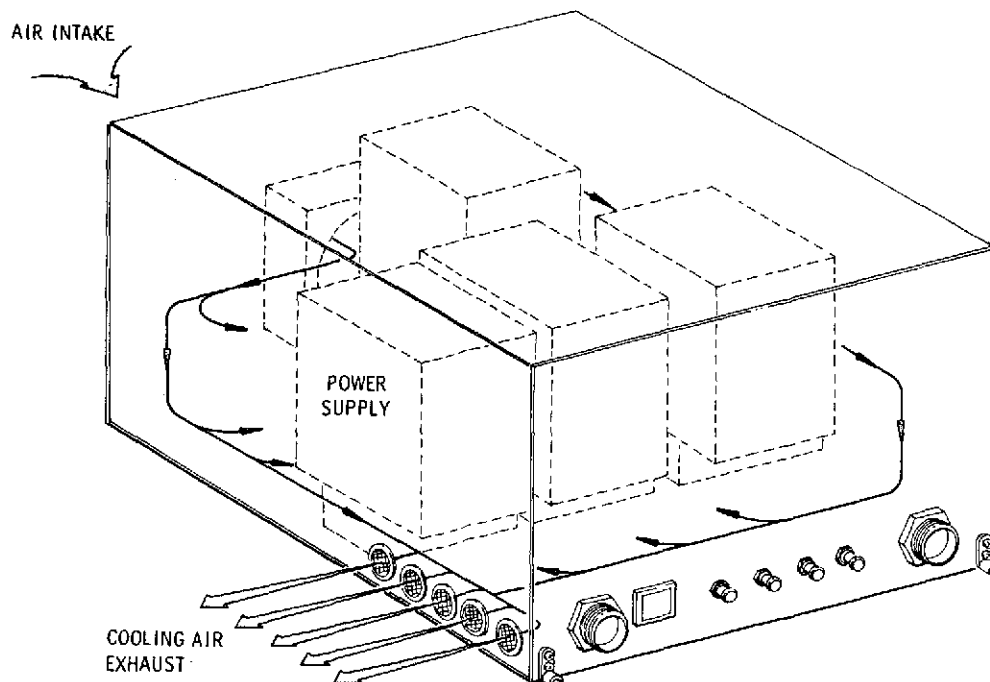
Figure 4-10. MMT/MTAR Power Supply

The front panel contains two hardwire connectors to interface with the Signal Processor and Receiver-Transmitter assemblies. A third hardwire connector is used to input prime power. A prime power fuse is located on the front panel. Each power supply output potential is protected with a resettable fuse also located on the front panel.

The cooling technique used for the power supplies is illustrated in figure 4-11. A single 115 VAC fan forces air from the rear of the assembly, through module heat sinks and out air exhaust holes located along the front sides of the chassis.

Pertinent mechanical specifications for the MMT/MTAR Power Supply include:

- | | |
|----------------|---------------------------------|
| • Size | 15.38W x 10.00H x 19.56L |
| • Cooling | Forced Air convection |
| • Weight | 65 pounds |
| • Construction | Sheet aluminum riveted assembly |



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Figure 4-11. Power Supply Cooling Technique

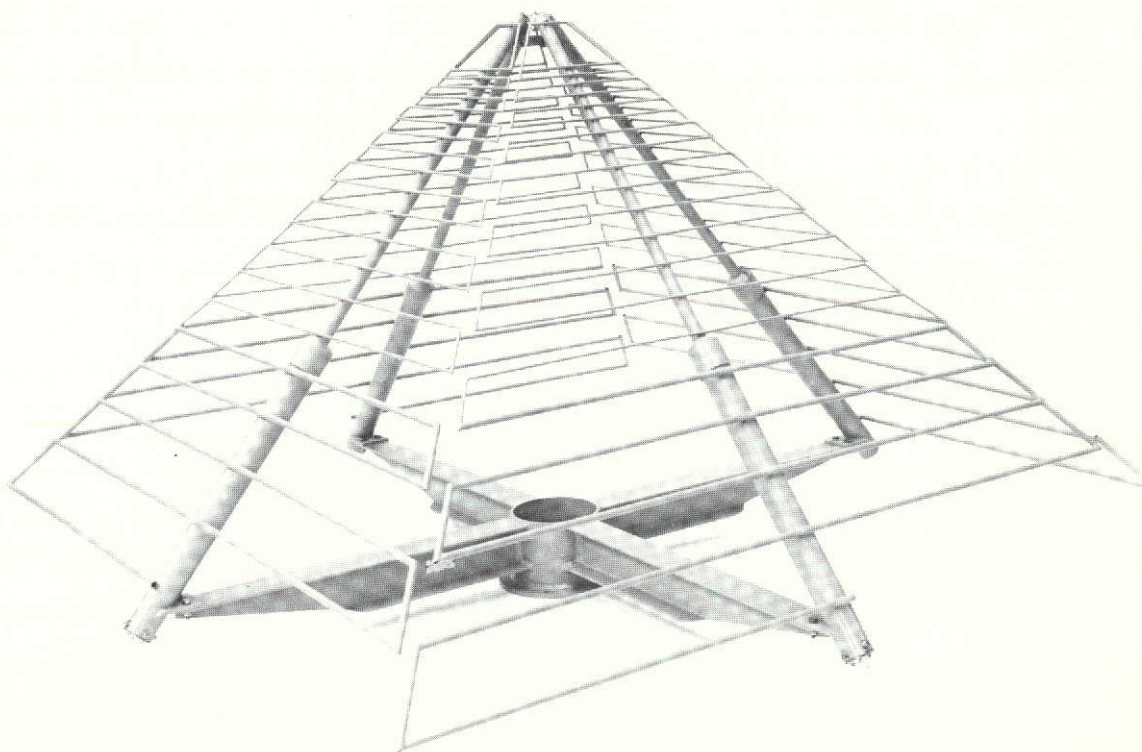
The power supply chassis is 15.38-inches wide x 10.69-inches high x 18.10-inches long. Structural and environmental design is based upon installation aboard a transport type aircraft. Basically, this unit is constructed of sheet aluminum with stiffening devices to support module weight. Since prepackaged power supply modules are used, wiring is accessible from the bottom of the unit. Each module has a forced-air heat exchanger which extends into the air plenum. A standard holddown arrangement is provided for mounting in a MS 91405 type mounting tray. Both top and bottom covers are provided with 1/4 turn fasteners to expedite installation and maintenance.

4.6 MTAR ANTENNA

The MTAR Antenna, shown in figure 4-12, was designed to provide hemispherical coverage and to be mounted on top of a mobile ground station. Some of the pertinent specifications for this antenna are listed below:

o	Type	Coincident Orthogonal Trapezoidal Logperiodic Array
o	Outputs	Dual 50 ohm Coaxial - N Type
o	Pattern	Unidirectional, Half Power Bandwidth for each Array
o	Construction	2-1/4" O. D. Tubing
o	Measurements	Base width = 50" Height = 34"

For simplicity and economy of design, two identical antenna structures capable of providing both the receiving and transmitting characteristics were used. The basic antenna is a trapezoidal log periodic array and is shown in figure 4-12. It consists of two periodic half-structures oriented at an angle ψ with respect to each other. These two half-structures form a balanced antenna which, when fed against each other from their vertex, radiate a unidirectional beam directed along the apex in the upward direction. This radiation is linearly polarized in the plane of the radiating elements. By placing a second pair of half-structures at right angles to the first, sharing a common apex, a second unidirectional linearly polarized beam can be obtained. By feeding each pair separately from coaxial inputs at the rear of the array, two independent, orthogonal, linearly polarized beams are obtained for polarization diversity. Circular polarization is obtained from the same array by combining the two linear pairs with a 90-degree phase shift between them.



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Figure 4-12. MTAR Antenna

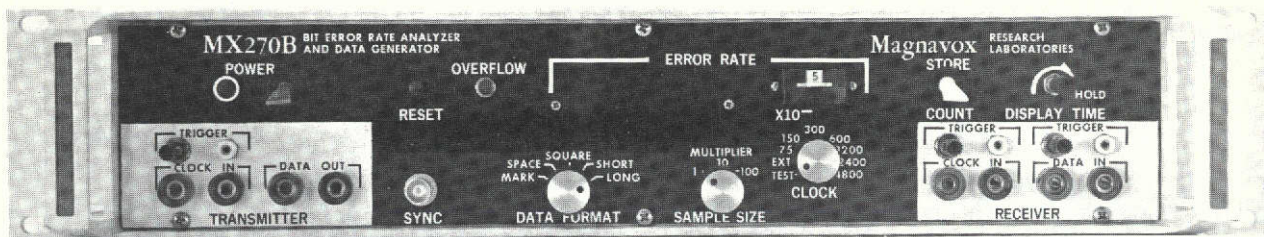
The radiation characteristics of the array are controlled by proper selection of the design parameters. For this application, it was desirable to have E and H plan beamwidths which were approximately equal. This array was designed to operate over the entire 126-402 MHz range and is pyramidal in shape with a square base of approximately 54 inches on a side and a base-to-apex height of approximately 36 inches.

4.7 TEST SUPPORT EQUIPMENT

The Test Support Equipment is identical for both the MTAR and MMT equipment. It consists of an MX 270 Bit Error Rate Analyzer and a Signal Monitor Box.

4.7.1 MX 270B BIT ERROR RATE ANALYZER

The MX 270B, shown in figure 4-13, provides a direct readout of error rate performance for digital communications modems. During operation, test data for the modem channel is clocked out of the MX 270B transmitter section at any rate up to 10 megabits per second. Similarly, the modem clocks data into the MX 270 receiver



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Figure 4-13. MX 270B Bit Error Rate Analyzer

section. This received sequence is compared bit-by-bit with the generated test sequence and thus the error rate is directly indicated. When a channel is tested on a simplex or full duplex basis, two MX 270B's are required.

The MX 270B is housed in a light weight 3-1/2 x 17 x 17 inch cabinet. The unit may be placed on a bench or rack mounted. Except for connectors, controls, and indicators, all electronic components are contained on a single board assembly. This assembly is constructed primarily of integrated circuits. Data and clock input/outputs are accessible from BNC connectors on the front panel.

4.7.2 SIGNAL MONITOR BOX

The MMT/MTAR Signal Monitor Box is shown in figure 4-14. This chassis provides easy access to status data. All data, data clocks and monitor signals are available from seven-way terminals. The audio input/output signals are available from standard military audio jacks used in most NASA applications. The hardwire interface cable between the monitor box and the signal processor units is also furnished with the unit. The signal monitor box is constructed from a standard 11 x 7 x 2 aluminum Bud chassis.

4.8 TEST BED CONFIGURATION

Major assemblies of both the MTAR and MMT equipment have been designed to mount together in a rack configuration as shown in figure 4-15. Allowing for two inch clearance between major assemblies, the equipment group can be mounted within four foot of panel space in a standard 19" rack. The Power Supply and Receiver-Transmitter assemblies would be hard mounted on trays within the rack. The Signal Processor would be mounted with isolators to a sliding tray. The isolators would provide protection from the anticipated aircraft environment and the sliding tray would allow convenient

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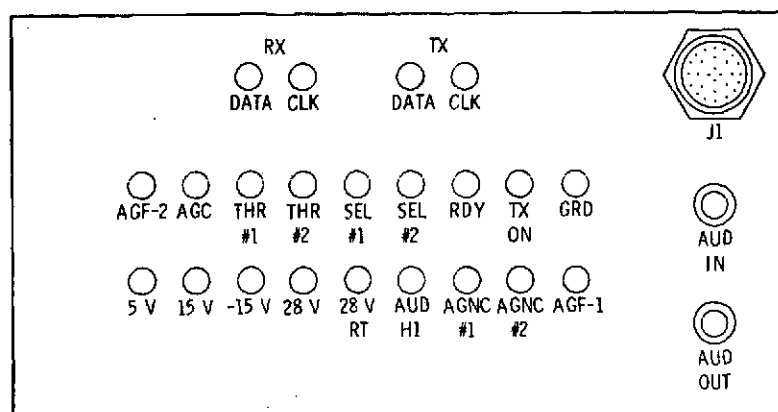


Figure 4-14. MMT/MTAR Signal Monitor Box

access to the PC assemblies within the Signal Processor. The Control-Display Panel (designed for mounting into a standard aircraft control-display panel) would mount with 1/4 turn fasteners into a special rack panel. Inter-assembly cables are supplied with the deliverable equipment in sufficient lengths to accommodate this configuration.

4.9 ENVIRONMENTAL CONSIDERATIONS

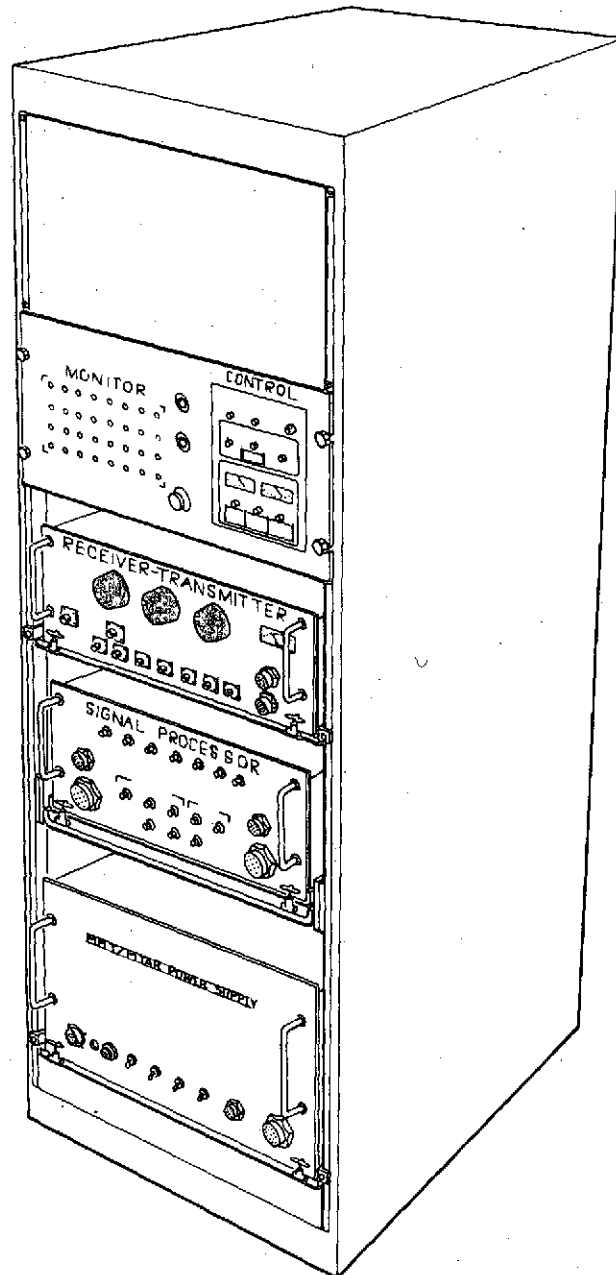
The TDRSS multimode transponder equipment has been designed to meet the functional requirements, when exposed to the service condition environments specified in table 4-2.

4.9.1 ELECTROMAGNETIC INTERFERENCE

The equipment was designed to operate satisfactorily in the intended installations without experiencing or creating abnormal EMI conditions. To accomplish this objective, care was taken to conform to established EMI/RFI design practices. Shielded components were connected via feed-through filters and coax lines.

Where RFI shielding was required in the board rack, a conductive plate was installed between boards with grounding provided by conductive bonding along the sides. As was noted earlier, the honeycomb sections in the signal processor units provide RFI protection between the rows of circuit boards while allowing a relatively unimpeded flow of cooling air from the forced-air cooling source.

Separate ground busses were maintained for signal neutral and case grounds. Provision was made to tie these busses to case ground inside the equipment. Potential sources of high-level interference and parasitics such as frequency dividers, local oscillators and circuits sensitive to interference were individually packaged in their own



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Figure 4-15. Rack Configuration for Both MMT and MTAR Equipment

Table 4-2. Environmental Service Conditions

Environment	STRESS LEVEL	
	Operating	Non-Operating
Thermal	32° F (0° C) to 122° F (50° C)	-25° F (-32° C) to 158F (65° C)
Relative Humidity	As low as 5% at 122° F (50° C); As High as 100% at All Temperatures From 32° F (0° C) to 85° F With Condensation At All Temperatures Lower Than 85° F (29° C)	Same as operating
Altitude	Up to 10,000 Feet Above Sea Level	Up to 25,000 Feet Above Sea Level
Vibration	5 Hz to 30 Hz: .02 inch double amplitude 30 Hz to 500 Hz: 1g	
Shock	As Encountered During Bench Handling	

shielded cases. Shielding at the chassis level was accomplished by utilizing overlapping riveted joints and oriented wire-silicone rubber gaskets at the top and bottom covers.

4.9.2 THERMAL CONSIDERATIONS

The cooling design was based on satisfying the requirements for installation in a transport aircraft of the C-121G type. Since the quality of the cooling air (cabin air) is suitable for direct flow through the electronics, a simple fan-filter assembly attached to the rear of both the signal processor and power supply was all that was required. Cooling air therefore enters the enclosures at the rear and exhausts at the sides just behind the front panel. No air passes directly out the front of the boxes where it could cause discomfort to an operator.

Honeycomb partitions allow free passage of air through the Signal Processor electronics. Power dissipation in the Signal Processor is approximately 125 watts. By using a fan which is rated at 110 CFM at free delivery, the airstream temperature rise does not exceed 5 degrees C.

In the Signal Processor, virtually all circuitry is packaged on plug-in printed circuit boards. Removal of the top cover provides access to all boards in the rack. Test points are provided along the top edge of most boards to assist in fault isolation. All circuit boards plug into edge connectors located in the lower portion of the case. Faulty boards can, therefore, be simply extracted and replaced. Removal of the bottom cover permits access to the connector back-plane wiring and the main wiring harness. Both covers utilize quick-turn fasteners to facilitate openings and closings. Since each module in the Power Supply is a self-contained unit, maintainability problems are minimized.

Removal of the Receiver-Transmitter unit cover (which also utilizes quick-turn fasteners) provides ready access to all elements of the electronics. Removal of the Control Display unit dust cover provides access to all components.

SECTION V

EQUIPMENT CHARACTERISTICS AND PERFORMANCE

This section contains a description of the electrical characteristics of the Multimode Transponder equipment. It sets forth the technical specification to which the equipment was designed and includes the theoretical calculations used to predict the performance of the equipment. In addition, it includes test data for the major parameters and performance characteristics.

5.1 EQUIPMENT SPECIFICATION

The technical requirements for the MMT and MTAR equipments (the two major equipment groups of the Multimode Transponder equipment) are presented in this section. These technical requirements were taken from an updated version of the contract Statement of Work which includes all contract modifications prior to delivery of equipment.

5.1.1 TECHNICAL REQUIREMENTS FOR THE MMT

5.1.1.1 Receiver Noise Figure

The receiver noise figure shall not exceed 3 dB.

5.1.1.2 Selectivity

The image rejection shall be at least 60 dB. Rejection of interfering signals more than 1.5 bandwidths away from the center frequency shall be at least 40 dB.

5.1.1.3 Inputs

The inputs to the transponder will be VHF command and ranging signals, telemetry data, clock signals, power, and operational housekeeping commands. The contractor shall supply simulators for necessary input signals which would normally be generated by the user spacecraft. Mode control and other transponder controls shall be provided by a contractor supplied control panel.

5.1.1.3.1 VHF Signals and Antenna

There will be two inputs from the VHF antenna, one for each of the polarization diversity channels. The VHF signals inputs will be command/tracking signal originating on the ground and relayed through a relay satellite. The contractor shall assume the EIRP of the relay satellite (ATS-F, GSFC Mark 1, and TDRS) to be 40 watts and its antenna gain 11.7 dB when the user spacecraft is at its maximum altitude of 5000 km. The VHF antenna associated with the multimode transponder shall be supplied by the contractor. This antenna shall be suitable for testing the transponder on the ground. The antenna will be an omni-directional polarization diversity antenna capable of operating in the following bands:

- 127.750 MHz
- 149 MHz
- 401 MHz
- 137 MHz

Manual switching between bands is permissible. This antenna shall also be capable of transmitting a signal in the frequency band of 136-138 MHz. The antenna shall be omni-directional right hand circularly polarized. The contractor shall also supply specification for an aircraft antenna at the completion of Phase I.

5.1.1.3.2 Command Signals

In all modes of operation except in Mode 3 (wideband PN), the transponder shall accept command signals from the ground and relayed through the relay satellite at rates of 100, 300, or 1000 bps. Provisions shall be made for switching between bit rates on the multimode transponder control panel.

5.1.1.3.3 Telemetry Data

In all modes of operation, the transponder shall accept telemetry data for transmission to the ground over the return link in the form of a binary bit stream at discrete rates of 0.3, 1, 3, or 10 kbps. Provisions shall be made for selecting a particular rate by manual selection at the control panel.

5.1.1.3.4 Voice Coding

A voice channel shall be incorporated into the transponder with all modes of operation. Pulse Duration Modulation technique shall be used. The design objective shall be for 98% intelligibility with a minimum C/NO of 42 dB per Hz. Tests shall be conducted using a 50 word phonetically balanced test.

5.1.1.3.5 Forward Error Encoding

The contractor shall provide forward error encoding in the transponder. The system provided shall be compatible with a convolutional decoder previously procured by GSFC.

Significant specifications for the GSFC decoder are:

- o Code type 1/2 code systematic or non-systematic
- o Constraint length - 8 to 48 bit
- o Quantization - 3 bit
- o Frame length - 512 to 4096 bits (50% information)
- o Frame synchronization - known contiguous sequence
- o Frame Synchronization code - 16 to 32 bit
- o Encoder Dump - equal to constraint length
- o Can handle up to 10 packed bits and 10 parity bits
- o Second parity bit must be complemented
- o Bit rates up to 50 Kbits (information 25 Kbits)

The forward error encoding shall be switched in and out by manual control.

5.1.1.3.6 Power

The Multimode Transponder is to operate properly when supplied power from a 58 Hz to 62 Hz source at 115 volts \pm 10%.

5.1.1.4 Outputs

The outputs of the transponder will be VHF telemetry data, VHF ranging signals, and simulated user spacecraft commands.

5.1.1.4.1 VHF Signals

The transponder shall deliver 1.0 watts of VHF power to the transponder antenna. The power output shall be capable of being attenuated 40 dB in 1 dB steps or by a continuously variable technique.

5.1.1.4.2 Ranging Signals

The transponder, when interrogated over the forward link by a received ranging signal, shall process this signal and retransmit over the return link a ranging signal suitable for the determination of system range and range rate at the ground station. The ranging system resolution in the absence of any communications channel noise (near infinite signal to noise ratio) shall allow range determination with a

maximum systematic error of 2.0 m and a maximum rms random error of 1.0 m, and shall allow determination of range rate with a maximum systematic error of 0.1 cm/sec and a maximum rms random error of 0.1 cm/sec.

5.1.1.4.3 Command Signals

The transponder shall demodulate the received command signal and deliver the resulting signal to an enclosed address decoder.

5.1.1.5 Modes of Operation

The transponder shall be capable of operating in three modes: conventional, narrowband PN and wideband PN. Provision shall be made for selecting the operating mode from the front panel.

In all modes (PN and Conventional) the transponder shall be capable of operating at 127.750 MHz, 149 MHz and 401 MHz. One frequency shall be received at a time and the band shall be manually selectable at the front panel.

5.1.1.5.1 Conventional Mode

Operation in the conventional mode for both the forward and the return links shall be in general conformance with the system planned for the GSFC Mark 1 TDRS.

Modulation-In the conventional mode, the modulation for both the forward and the return links shall be PSK with a phase shift of $\pm 90^\circ$.

5.1.1.5.2 Narrowband PN Mode

Operation in the narrowband PN mode, for both the forward and the return links, shall be in general conformance with the system planned for the GSFC Mark 1 TDRS. The narrowband PN mode shall be usable for receiving commands and ranging signals over the forward link, and for transmitting telemetry data and ranging signals over the return link.

Chip Rate-Two different chip rates shall be available for the narrowband PN modulation consistent with bandwidth occupancies of 50 and 130 KHz. These rates shall be selected by operational housekeeping command from the ground through the user spacecraft housekeeping command system, and shall be available for the forward and return links independently in any combination.

Multiple Access-Consideration shall be given to the requirement that several user spacecraft utilize the same carrier frequency for the return link simultaneously, discrimination between signals being achieved by the use of orthogonal or quasi-orthogonal coding and of proper address codes.

5.1.1.5.3 Wideband PN Mode

Operation in the wideband PN mode will be for the return link only, and shall be in general conformance with the system planned for the GSFC Mark 1 TDRS. The wideband PN mode shall be usable for the transmission of telemetry data and for the retransmission of ranging signals over the return link.

Chip Rate-The chip rate for the wideband PN modulation shall be chosen consistent with a fully loaded system bandwidth occupancy of 1.5 MHz.

Frequency-In the wideband PN mode, the carrier frequency transmitted over the return link shall be 137 MHz.

Multiple Access-In the wideband PN mode, all 20 user spacecraft (in actual TDRSS operation) will transmit signals over the return link to the relay satellite simultaneously in a shared 1.5 MHz band. Provisions for multiple access must therefore be made through the use of orthogonal or quasi-orthogonal coding and of proper address codes.

5.1.1.6 Test Equipment

The contractor shall supply two MX-270 Bit Error Rate Analyzers for the purpose of (1) generating the required data rates, or (2) for measuring received data error rates.

5.1.2 TECHNICAL REQUIREMENTS FOR THE MTAR

5.1.2.1 Introduction

The MTAR is to perform the same function radio communication wise as the conceptual transmitter and receiver aboard the TDRS. However, their principle function is to supply to and receive signals from the multimode transponder in a number of test configurations in which the MTAR are always ground based. The MTAR are to be fully compatible with the Multimode Transponder. Since this equipment is to be utilized in engineering test only, it is to be fabricated using the best commercial practices.

In the description to follow the values for various parameters are representative only; the actual values and numbers will be dictated by the results of the design study for the multimode transponder.

The transmitter will supply a signal in the frequency bands utilized by the multimode transponder at a level of one watt to a 50 ohm load which represents an antenna. This signal shall be capable of being modulated according to the following modes of operation:

- Pseudo-random (PN) bit stream which has been modulo-2 added with NRZC data modulates the carrier according to PSK.
- Conventional mode (PSK) in which NRZC data modulates the carrier as PSK in a straightforward manner.

In the PN mode the PN code must have good auto- and cross-correlation properties so that the correlator noise from the multimode transponder will cause a minimum false alarm rate before synchronization is established. Measurement of range will be facilitated by measuring the transit time of code sequences. Additional ambiguity resolution, if required, will be supplied by the channel. Range is determined to a resolution corresponding to a small fraction of PN bit (chip).

In the PN mode, pulses derived from the all-ones vector in the transmitted signal and the all-ones vector in the received and demodulated signal together with auxiliary range ambiguity signals from the data channel will be accessible to periphery equipment. The contractor will produce an unambiguous range gate from these signals and apply a gated signal with appropriate characteristics to a counter and printer unit to read out range in terms of round trip range signal delay expressed as counts of the gated signal.

5.1.2.2 Transmitter Signal Stability

The phase, amplitude and frequency stability of the transmitter signals and the modulation thereon shall be, in the absence of any type of interfering signal including additive channel noise, sufficient to accomplish the following:

1. Supply command data to the Multimode Transponder (MMT) with a 30 dB SNR over the dynamic range of the system.

2. Supply range signals to the MMT which when processed by the MMT and returned to the ground receiver will cause a range uncertainty of 1.0 meter maximum in a one second averaging time.
3. Supply signal which can be synthesized back to the original carrier component in the MMT and subsequently at the output of the ground receiver sufficient to providing a range rate signal having an uncertainty of 0.1 cm maximum in 10 seconds averaging time.

5.1.2.3 Transmission Power Levels

The ground transmitter shall be capable, in the PN and PSK modes, of supplying 1 watt rms to a 50 ohm cable terminated with a 50 ohm lead.

The transmitter output level shall be capable of being reduced by 40 dB in dB steps or in a continuously variable fashion calibrated to 1 dB.

5.1.2.4 Transmitter Output Frequency

The frequency of transmission shall be compatible with the Multimode Transponder.

5.1.2.5 Transmitter Signal Formats and Modulation

The ground transmitter will supply a data clock signal to the data source. A commercial instrument is envisioned as the data source. The data source is to supply NRZC data of various types including a random bit stream to the ground transmitter.

5.1.2.5.1 PN Mode

In the PN mode this data stream is modulo-2 added with the internal PN signal. This PN signal is applied to a PSK modulator with the result that the modulation is biphase Differential Phase Shift Keyed (DPSK).

5.1.2.5.2 PSK Mode (Conventional)

In the PSK mode the input data stream PSK modulates directly a carrier component such that the result is again DPSK. The baseband modulation signal in all modes is to be applied to an external connector for purposes of interfacing with other transmitters.

5.1.2.5.3 PN Code

The PN code generated in the ground transmitter shall be fully compatible with the requirements for the Multimode Transponder. Representative values for the parameters associated with this code for the forward link are:

- Chip Rate - 102.4 kcps (150 KHz BW)
- Sequence Length - 4095 chips
- Type Code - Maximal linear sequence with optimum auto - and cross-correlation properties.

In addition to a channel bandwidth of 150 KHz, 50 KHz and 1.5 MHz with appropriate chip rates are being considered.

5.1.2.6 Receiving System Sensitivity (All Modes)

The system being simulated here, i.e., User Spacecraft/TDRS VHF communication links, will have at times, because of RFI and multipath, a negative communication margin. Therefore, it is required that the ground receiver system have both an acquisition and operating sensitivity which is close to the theoretical optimum. Because the Multimode Transponder will code its transmitted signal with forward error control the theoretically optimum sensitivity in the data link for a bit error (BER) of 10^{-5} is specified as: $E/N_0 = 5$ dB where N_0 includes all extraneous signals including receiver noise, sky noise, RFI, and multipath effects. The sensitivity of the ground receiver shall be within 2 dB of the theoretical optimum for both acquisition and operation based upon the E/N_0 relationship as described above over the dynamic range of the receiver (specified below).

5.1.2.7 Ground Receiver Dynamic Range

At the minimum bit rate of 300 bps and minimum system noise temperature of 600 degrees K the threshold input signal level is -140 dBm. The maximum received signal level, with some exaggeration of the MMT user Transponder power transmitting capabilities is -100 dBm. Therefore, the dynamic range of the ground receiver shall extend from -100 dBm to -140 dBm.

5.1.2.8 Acquisition Time of the Ground Receiver

The acquisition time for the PN mode without diversity, shall be a maximum of 50 seconds with a desired acquisition time being ten seconds or less at all received signals and formats where the system, after acquisition, can output data

with a bit error rate (BER) no greater than 10^{-5} . In view of the plus and minus 8 KHz of doppler variations on the received signal and the requirement for maintaining sensitivity during acquisition, a doppler processor will be used.

5.1.2.9 Ground Receiver and Signal Processor Bandwidths

The bandwidths involved with the ground receiving function are to be compatible with the signal emitted by the Multimode Transponder for the various modes.

5.1.2.10 Polarization Diversity

Polarization diversity reception will be utilized in this ground receiver. The signals will be combined optimally according to inverse ratio squared.

5.1.2.11 Data Output

The received and demodulated data stream shall be applied to a connector for external accessibility. The voltage level of this data stream shall be the standard logic format utilized throughout the system. It is assumed for the PN mode that throughout the MTAR and Multimode Transponder the data rate is coherent with the PN sequence rate such that bit synchronization is readily available once code synchronization is established. The contractor shall utilize the coherency in establishing bit synchronization and will process the data by a matched filter such as an integrate and dump circuit before applying to the output connector.

5.1.2.12 Range Signals (PN Mode)

The range signals will be supplied in the form of start and stop pulses. These signals are fed into an internal counter equipped with a printer such that a tabulation of two-way range in seconds is produced. Multiplying these numbers by a determinable constant results in the actual range. The gate start pulse is derived from the all-ones condition in the ground transmitter. The gate stop pulse is derived from the all-ones condition of the local PN code signal which is synchronized through a 1 Hz code tracking bandwidth to the received PN code signal. Tabulating range more often than at one second intervals results in redundancy; therefore, the counter will be arranged to make only one counting operation per second. Epoch timing will be arranged by synchronizing the PN code sequence in the ground transmitter to the station time standard.

5.2 CALCULATED PERFORMANCE

The expected performance of the Multimode Transponder and associated ground equipment has been calculated and curves have been constructed to show the theoretical performance including implementation losses in this section.

5.2.1 DATA RECOVERY PERFORMANCE

Data recovery performance for the Multimode Transponder departs from the theoretical curves for DCPSK detection for two important reasons. The first, which is less significant, is the imperfect carrier tracking. The second, which is the major reason, is the loss due to RC data filtering in the side integrators of the demodulator, prior to I and D filtering.

5.2.1.1 Imperfect Carrier Tracking Losses

Imperfect carrier tracking is interpretable in terms of a phase error in the carrier reference. A phase error ϕ in the reference changes the in-phase channel voltage by $\cos \phi$ with a noise contribution of $\sin \phi$. Thus, the bit energy to noise density varies as $(\cos \phi + \sin \phi)^2$. For small phase errors the above is approximated by $(1 + \phi)^2$. The probability of bit error conditional on the reference angle error ϕ is given by:

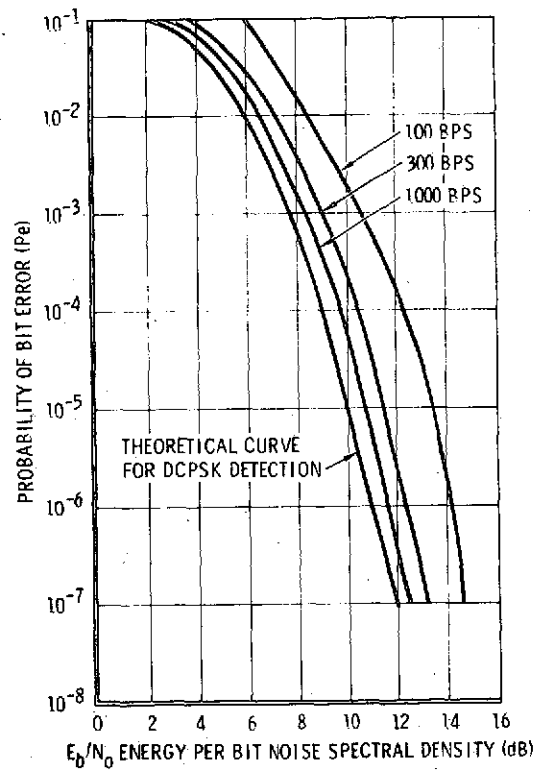
$$P_e(\phi) = \frac{\exp[-E_b/N_o (1 + \phi)^2]}{2 \quad 2 E_b/N_o (1 + \phi)}$$

The probability of bit error is found from the integral given by:

$$P_e = \int_{-\infty}^{\infty} P_e(\phi) P(\phi) d\phi$$

Upon integration, with the appropriate substitution for the approximately Gaussian variable $P(\phi)$, we get $P_e [\exp - (2E_b/N_o + 1) \frac{\sigma^2}{2}]$. Where σ^2 is the mean square value of the noise in the carrier loop and P_e is the probability of error for a DCPSK system with a perfect reference. On a low pass equivalent basis, since B_L (loop noise bandwidth) is a low pass one sided bandwidth, there is an effective processing gain in the loop equal to $10 \log \frac{\text{Data Rate}}{B_L}$. Thus, white gaussian noise, after filtering by the

carrier loop is $-(E_b/N_0 + 10 \log \frac{DR}{BL})$ relative to unit signal power which is equivalent to σ^2 . The E_b/N_0 is obtained from the theoretical curve at the particular point where the degradation is required to be known. Using the equation for P_e , and the relationship above for σ^2 , the E_b/N_0 degradation due to imperfect carrier tracking is obtained for a data rate of 100 bps, 300 bps and 1000 bps. This is shown in figure 5-1.



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Figure 5-1. P_e vs E_b/N_0 for DCPSK with Imperfect Carrier Tracking

5.2.1.2 RC Data Filtering Losses

The degradation due to RC data filtering is essentially obtained from the work done by J. Jay Jones [1]. He provides a relationship of probability of error vs E_b/N_o for a single pole RC filter for CPSK with the 3 dB RF bandwidth and data rate as variable parameters.

For the design criteria of the 3 dB bandwidth being equal to the data rate, a relationship of P_e vs E_b/N_o can be obtained for the single pole RC filter. The relationship for P_e vs E_b/N_o for a single pole RC filter for DCPSK is shown in figure 5-2.

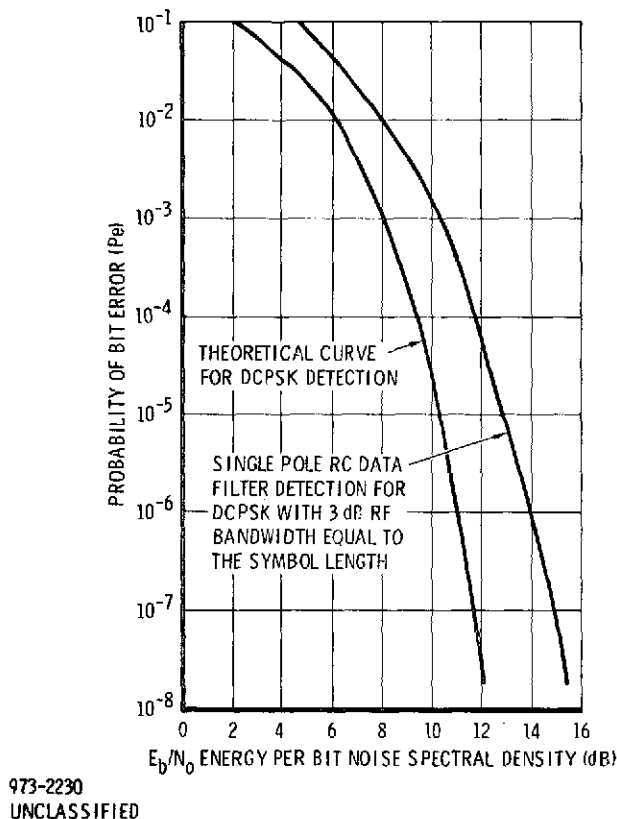
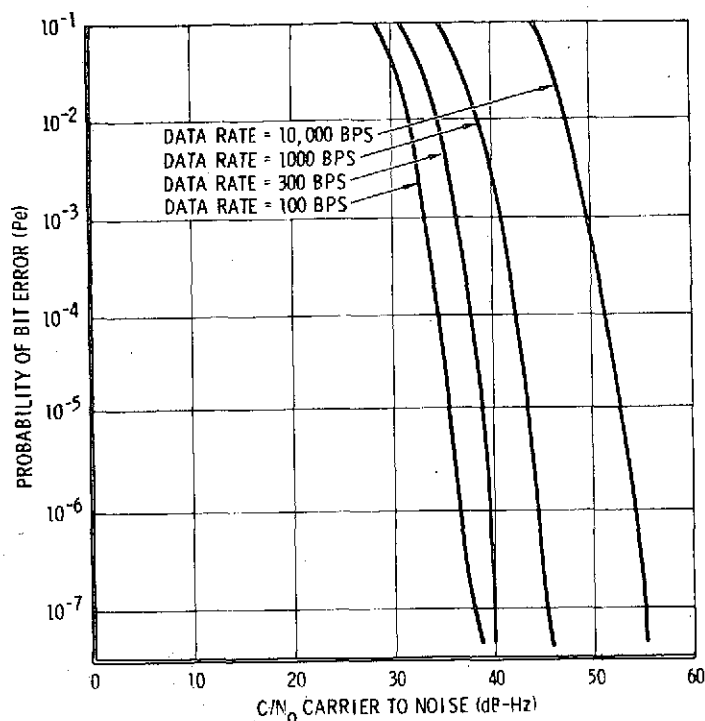


Figure 5-2. P_e vs E_b/N_o with RC Data Filtering for DCPSK

Combining the degradation from data filtering and imperfect carrier tracking provides the required C/N_o for the specified P_e at various data rates. This is shown in figure 5-3.

[1] Jones, Jay, J. "Filter Distortion and Intersymbol Interference effects on psk signals", IEEE Transactions on Communication Technology, Vol. COM-19 No. 2, April, 1971.



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Figure 5-3. Expected Multimode Transponder Data Recovery Performance

It should be pointed out that data demodulation performance improves by approximately 3 dB when both diversity receivers are tracking and their data outputs are combined. Also during a transpond mode of operation, the return link performance will be reduced somewhat if the signal source (MMT transmitter) is noisy due to phase sitter of the tracking reference.

For the PN modes of operation, a 1 dB loss in performance can be expected due to imperfect code tracking at threshold. Also, since the data is reclocked with the PN code clock, quantization losses can be expected on the order of 1 dB for code/data clock ratios of 10/1 and 2 dB for code/data clock ratios of 3/1.

5.2.2 RANGE MEASUREMENT

The expected two-way ranging performance for the Multimode Transponder has been calculated. Bandlimiting and tracking S/N losses have been considered.

The delay lock loop rms range tracking error may be written as:

$$\sigma \Delta \tau_{\text{rms}} = \frac{1}{\sqrt{\frac{S}{2N_o B_L}}} \frac{R(0) - R(2\tau_d)}{2R'(\tau_d)}$$

Where:

B_L = one-sided loop noise bandwidth

N_o = one-sided noise power density

S = average signal power

τ_d = jitter time displacement in bits

The bandlimited autocorrelation junction used above can be shown to be given by:

$$R(\tau_d) = \frac{1}{\pi} \left[\frac{2}{B} \cos B\tau_d (\cos B - 1) - 2\tau_d \text{Si}(B\tau_d) \right. \\ \left. + (1 + \tau_d) \text{Si}[B(1 + \tau_d)] + (1 - \tau_d) \text{Si}[B(1 - \tau_d)] \right]$$

Where:

$$B = 2 f_r T$$

f_r = one-sided bandwidth of the receiver filter

T = PN code bit width

The rms range tracking error versus the carrier to noise ratio for a loop B_L of 4 Hz, a $f_r = 1.5$ MHz and for two-way ranging is shown in figure 5-4 for a time jitter displacement = .5 bits. The chip rates of 34.133 kcps, 102.4 kcps and 1024 kcps are included for both the uplink and downlink. The rms range error is also shown for an uplink of 102.4 kcps and a downlink of 1024 kcps.

5.2.3 RANGE RATE TRACKING

The theoretical range rate accuracy of carrier doppler is dependent on the loop signal-to-noise ratio neglecting dynamics. From a known carrier frequency, the

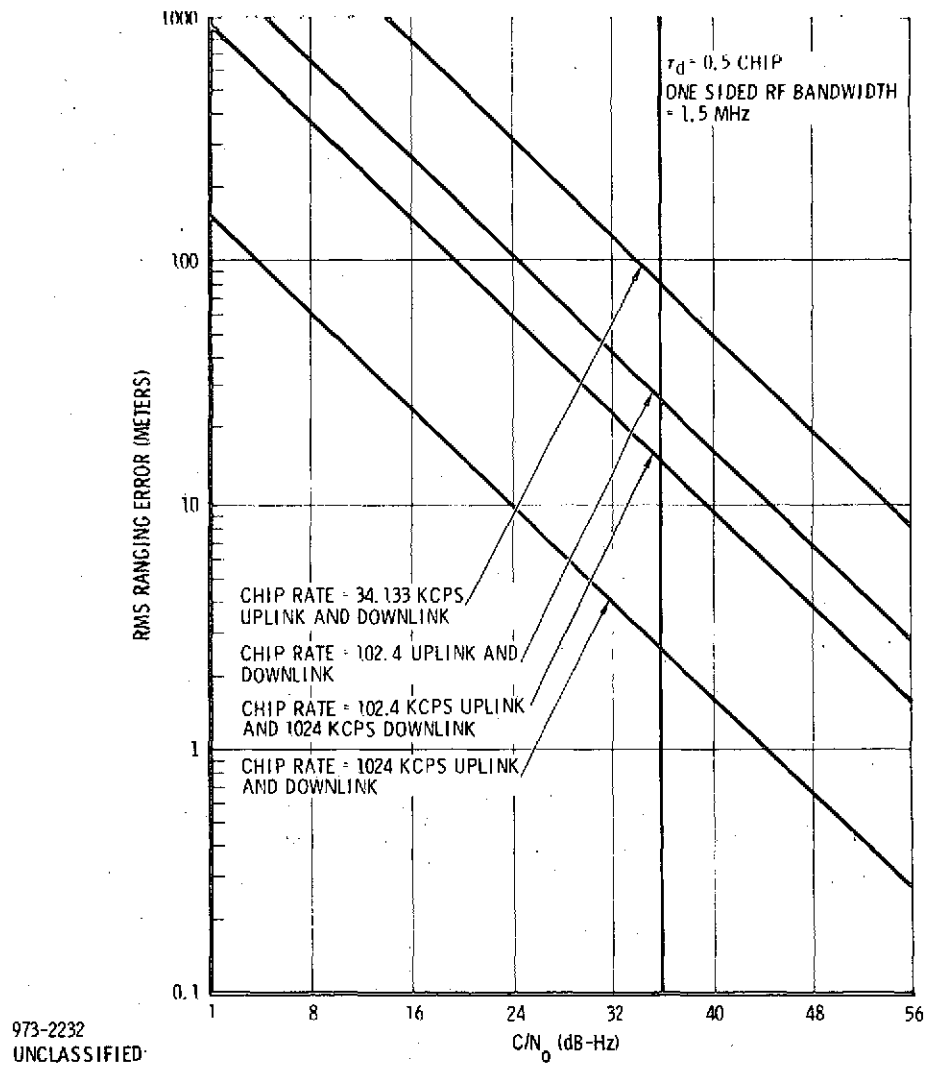


Figure 5-4. RMS Range Tracking Error vs Carrier to Noise Ratio for Two-Way Ranging

doppler measurement is made by taking the ratio of the total phase increment (relative to a reference oscillator) divided by the time interval τ . The phase is, therefore, measured first at the start of the interval and then at the end. If $B_L \tau \gg 1$, the two-phase measurements have independent errors and the rms range rate tracking error can be written as:

$$\sigma \Delta v = \frac{C}{2 f_o} \sqrt{\frac{2 N_o B_L}{S}}; B_L \tau \gg 1$$

Where:

C = velocity of propagation

f_o = carrier frequency

τ = interval time

For a carrier frequency of 137 MHz, a B_L of 40 Hz, and an interval time of 1 sec, the relationship of one-way rms range rate error versus carrier-to-noise ratio is shown in figure 5-5.

Note that this is one-way range-rate error. The actual two-way performance would have to account for the cumulative carrier noise error in both the forward and return links divided by two.

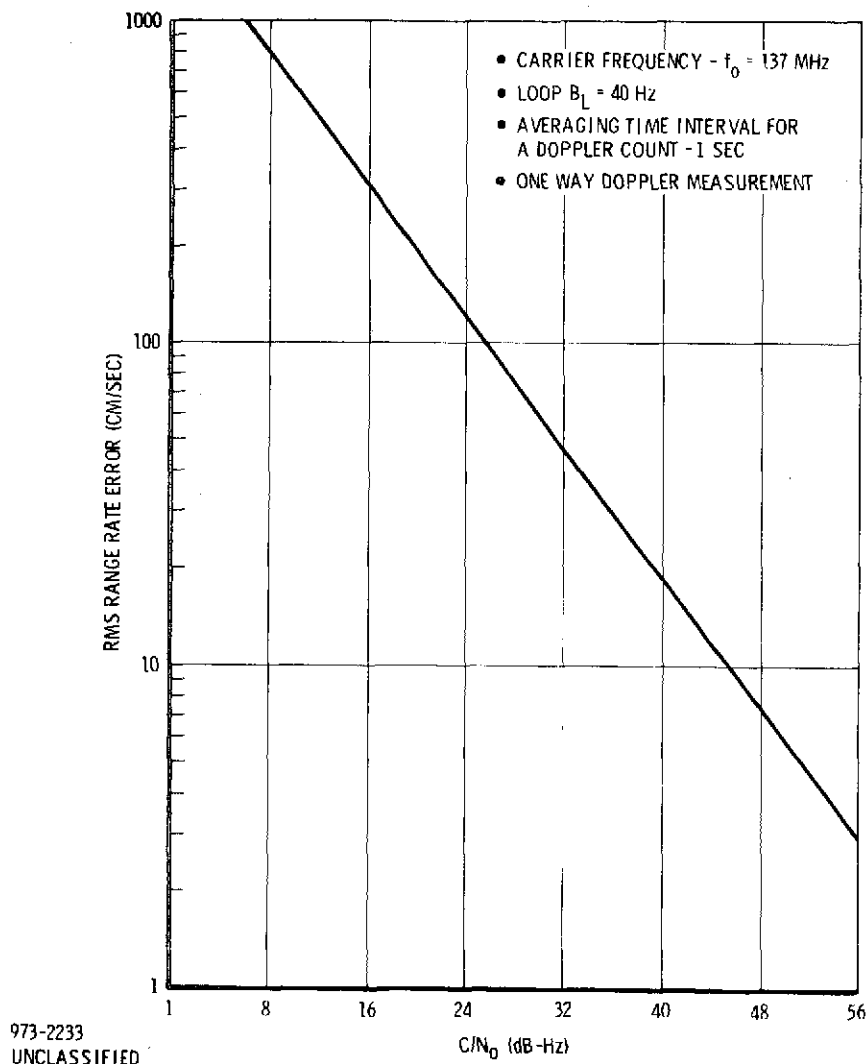


Figure 5-5. RMS Range Rate Error vs Carrier-to-Noise Ratio

5.3

MEASURED RECEIVER AND TRANSMITTER CHARACTERISTICS

Test data for pertinent receiver and transmitter parameters are presented in this section along with the data, test conditions, and test setups also shown.

5.3.1 RECEIVER SELECTIVITY

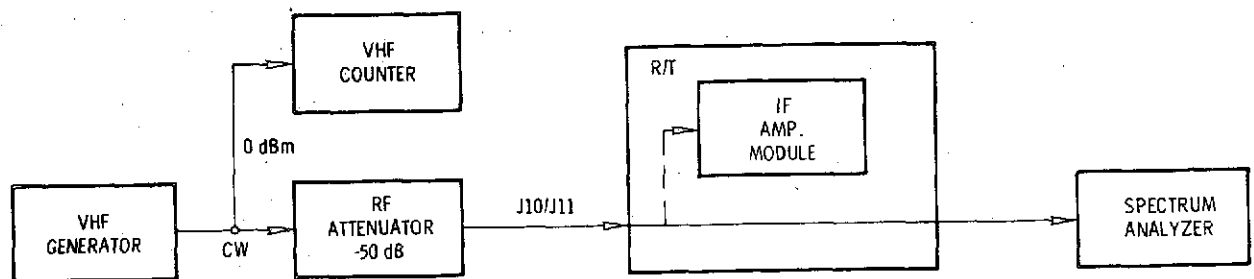
RF bandwidths of the Multimode Transponder receivers, determined primarily by quadriplexes and other bandpass filtering prior to the first IF, is indicated by the receiver selectivity data shown in table 5-1. Figure 5-6 shows the test setup used to obtain the receiver selectivity data.

5.3.2 RECEIVER IMAGE REJECTION

Image frequencies for each of the four multimode transponder RF frequencies are shown in table 5-2 along with the image rejection levels at the second IF output of each receiver. In each case, a CW generator signal was inserted at the RF output to the receiver at the desired RF frequency and the resulting response was measured at the 2nd IF. The image rejection level is referenced to an input signal at center frequency.

5.3.3 TRANSMITTER SPURIOUS NOISE

The spurious noise levels at the output of the multimode transponder transmitters are shown in table 5-3. The spurious levels are referenced with respect to the output signal level.



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Figure 5-6. Selectivity Test Setup

Table 5-1. Receiver Selectivity

RCVR #1	f_H/f_L	FREQUENCY (MHz)			
		1 dB	3 dB	6 dB	40 dB
<u>MTAR</u>					
137 MHz	f_H	139.0	139.4	139.8	141.6
	f_L	136.5	134.6	134.4	132.6
<u>MMT</u>					
127.750 MHz	f_H	127.9	128.5	129.0	131.2
	f_L	124.6	124.4	123.2	121.9
129 MHz	f_H	151.9	152.9	153.4	155.7
	f_L	145.8	144.3	144.4	142.6
401 MHz	f_H	403.9	405.1	406.3	411.7
	f_L	398.0	397.1	396.1	387.9
RCVR #2	f_H/f_L	FREQUENCY (MHz)			
		1 dB	3 dB	6 dB	40 dB
<u>MTAR</u>					
137 MHz	f_H	139.2	139.4	139.8	141.8
	f_L	134.6	134.4	133.8	132.2
<u>MMT</u>					
127.750 MHz	f_H	128.8	129.2	129.5	132
	f_L	125.0	124.3	124.0	122.4
149 MHz	f_H	152.0	153.0	153.6	156.1
	f_L	146.3	144.7	144.2	142.1
401 MHz	f_H	404.0	405	406.3	415.5
	f_L	398.0	396.6	395.1	391.4

Table 5-2. Receiver Image Rejection

RCVR #1	IMAGE FREQ. (MHz)	IMAGE REJECTION (dB)
<u>MTAR</u> 137 MHz	23.0	78
<u>MMT</u> 127.750 MHz 149 MHz 401 MHz	7.75 13.50 265.5	> 80 > 80 >100
RCVR #2	IMAGE FREQ. (MHz)	IMAGE REJECTION (dB)
<u>MTAR</u> 137 MHz	23.0	78
<u>MMT</u> 127.750 MHz 149 MHz 401 MHz	7.75 13.50 265.5	> 80 > 80 >100

Table 5-3. Transmitter Spurious Noise

	SPURIOUS OUTPUT LEVEL	
<u>MTAR XMTR #1</u>	XMTR #1	XMTR #2
127.750 MHz	-40 dB	-36 dB
149.000 MHz	-34	-38
401.000 MHz	-37	-37
<u>MMT XMTR #1</u>		
137.000 MHz	-47	-46

5.4 PERFORMANCE TEST DATA

The measured performance of the multimode transponder equipment in the areas of: (1) data recovery; (2) range measurement; and, (3) range rate measurement are presented in this section. Performance was evaluated by measuring data error rate, range error or range rate error for given C/N_o ratios. The C/N_o ratios were calculated from the following relationships:

$$N_o = -174 \text{ dBm} + \text{N. F.}$$

$$C = \text{Tx} - \text{Attn}$$

$$C/N_o = (\text{Tx} - \text{Attn} + 174 - \text{N. F.}) \text{ dB}$$

where:

$$N_o = \text{Thermal Noise/Hz (dBm)}$$

$$\text{N. F.} = \text{Noise Figure (dB)}$$

$$C = \text{RF Carrier (dBm)}$$

$$\text{Tx} = \text{Xmtr Output (dBm)}$$

$$\text{Attn.} = \text{Attenuation (dB)}$$

For each test, thermal noise was used as a jamming source and the desired C/N_o ratio was selected by presetting a variable attenuator. Each transmitter output was adjusted to -30 dBm and the desired C/N_o ratio was obtained by presetting the variable attenuators to a value calculated from the following relationship:

$$\text{Attn.} = (174 - 30 - \text{N. F.} - C/N_o) \text{ dB}$$

5.4.1 DATA RECOVERY

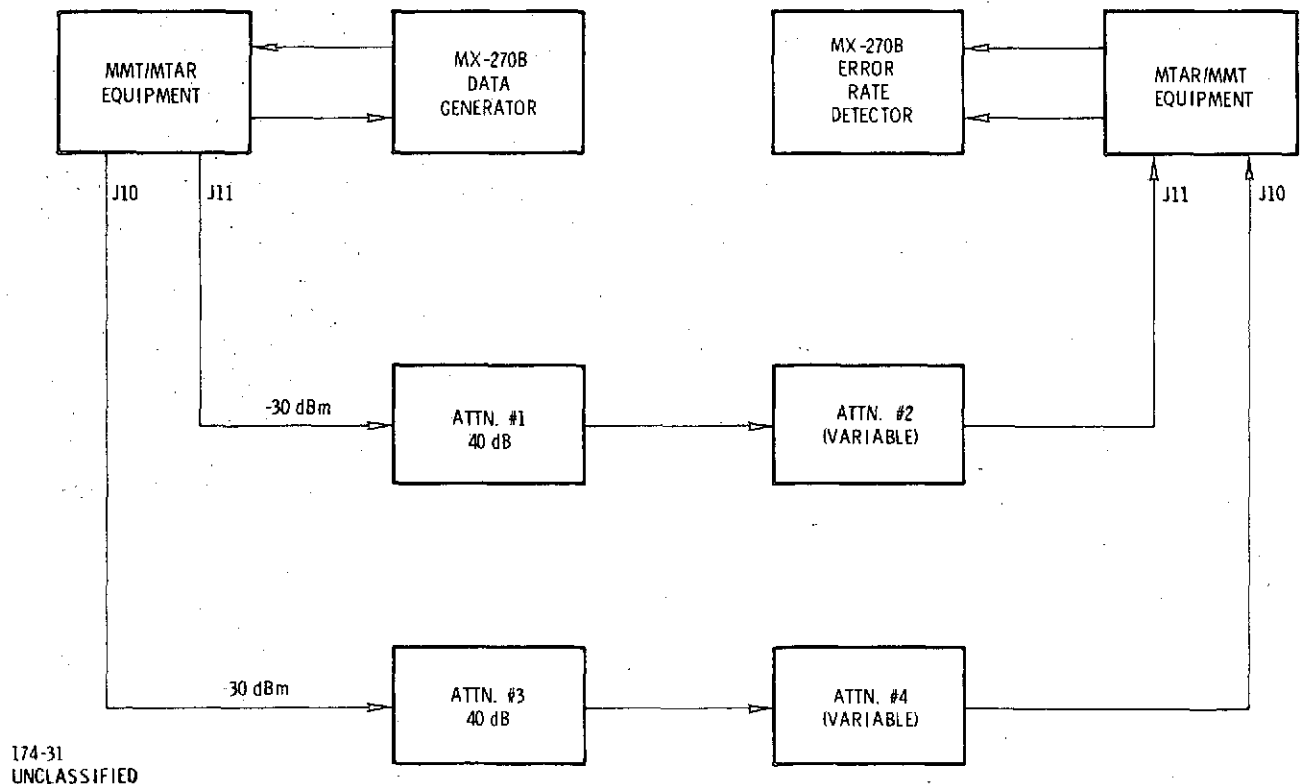
Data recovery performance for twelve different modes of operation are presented in this section. Performance is shown for the following forward link modes:

Link Mode	Forward only
Frequency	127.750 MHz
PN Chip Rate	102.4 KCPS
Data Rate	300 or 1000 BPS
Modulation	PN or PSK
Receiver No.	1, 2, both

Performance is shown for the following return link modes:

Link Mode	Return only
Frequency	137 MHz
PN Chip Rate	102.4 KCPS
Data Rate	1000 or 3000 KCPS
Modulation	PN or PSK
Receiver No.	1, 2, or both

The test setup used for these tests is shown in figure 5-7.



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Figure 5-7. Data Recovery Test Set-Up

Table 5-4. Data Recovery (PSK-RCVR #1 - Forward Link)

Data Rate	C/N ₀ (dB)	Signal Level	Error Rate (@ x 10 ⁻⁴)	Sample Time (Seconds)
300 bps	36	-131	0.0	330
	35	-132	0.4	
	34	-133	1.4	
1000 bps	40	-127	0.0	100
	39	-128	0.9	
	38	-129	3.8	

Table 5-5. Data Recovery (PSK-Combined Receivers - Forward Link)

Data Rate	C/N ₀ (dB)	Signal Level	Error Rate (@ x 10 ⁻⁴)	Sample Time (Seconds)
300 bps	33	-134	0.4	330
	32	-135	0.2	
	31	-136	1.0	
1000 bps	36	-131	.6	100
	35	-132	1.2	
	34	-133	8.6	

Table 5-6. Data Recovery (PN-RCVR #2 - Forward Link)

Data Rate	C/N ₀ (dB)	Signal Level	Error Rate (@ x 10 ⁻⁴)	Sample Time (Seconds)
300 bps	36	-131	0.0	330
	35	-132	1.8	
	34	-133	5.2	
1000 bps	40	-127	0.2	100
	39	-128	0.8	
	38	-129	7.0	

Table 5-7. Data Recovery (PSK-RCVR #2 - Return Link)

Data Rate	C/N ₀ (dB)	Signal Level	Error Rate (@ x 10 ⁻⁴)	Sample Time (Seconds)
1000 bps	40	-129	0.0	100
	39	-130	0.6	
	37	-131	0.2	
3000 bps	45	-124	0.0	33
	44	-125	0.6	
	43	-126	2.4	

Table 5-8. Data Recovery (PN-RCVR #1 - Return Link)

Data Rate	C/N ₀ (dB)	Signal Level	Error Rate (@ x 10 ⁻⁴)	Sample Time (Seconds)
1000 bps	42	-127	0.0	100
	41	-128	0.4	
	39	-129	3.0	
3000 bps	50	-119	0.2	33
	49	-120	1.8	
	48	-121	7.0	

Table 5-9. Data Recovery (PN-Combined Receivers - Return Link)

Data Rate	C/N ₀ (dB)	Signal Level	Error Rate (@ x 10 ⁻⁴)	Sample Time (Seconds)
1000 bps	40	-129	0.0	100
	39	-130	0.2	
3000 bps	48	-121	0.0	33
	47	-122	1.4	
	46	-123	3.8	

5.4.2 RANGE MEASUREMENT PERFORMANCE

Range measurements are performed in a full duplex mode of operation using a computing counter to compute the range delay in nanoseconds. Both RMS and mean ranging performance are shown for the following modes:

Link Mode	Transpond
Modulation Mode	PN
PN Chip Rate	102.4 KCPS
Forward Frequency	127.750 MHz
Data Rate	300 BPS
Data Generator	Pseudo-random
C/N ₀	42 or 82 dB

The test setup for the range measurement performance tests is shown in figure 5-8. Table 5-10 shows the results for RMS ranging error performance using a 100 sample average.

Table 5-11 shows the results for mean ranging error performance using a 100 sample average at a C/N₀ = 82 dB.

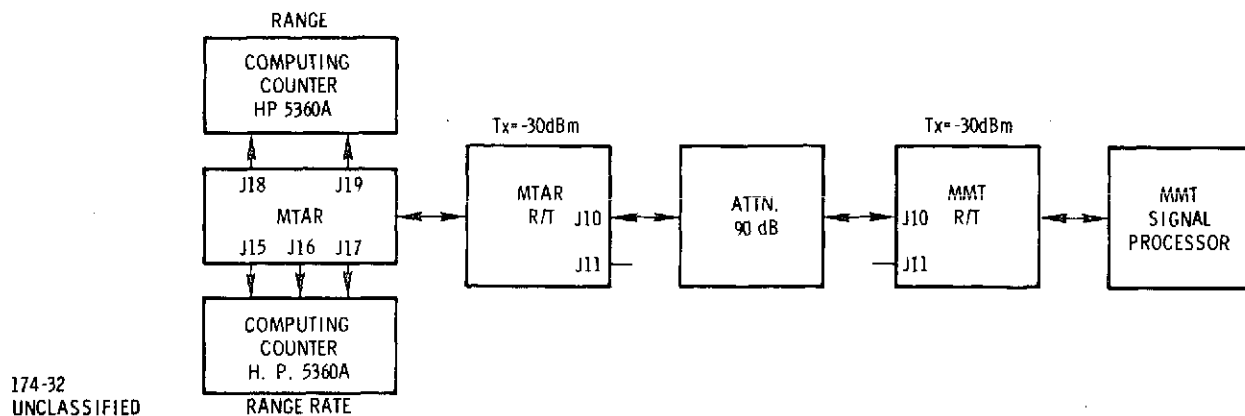


Figure 5-8. Range and Range Rate Measurement Test Setup

Table 5-10. RMS Ranging Error Performance

Signal/Noise (C/N ₀)	Trial No.	RMS Error (μ _s)
42 dB	1	99.501
	2	90.227
	3	93.169
82	1	2.9584
	2	2.9347

Table 5-11. Average Ranging Error Performance

Condition	Trial No.	Delay (μ _s)
With no RF cable	1	2.4468
	2	2.4411
	3	2.4379
	4	2.4380
	Average	2.441
With 100' cable	1	2.5579
	2	2.5584
	3	2.5578
	Average	2.558
Measured range		117 feet

5.4.3 RANGE RATE MEASUREMENT

Range rate measurements will be performed in a full duplex mode of operation using a computing counter to measure range rate in Hz. RMS range rate performance is shown for the following mode:

Link	Transpond
Modulation	PSK
Forward Frequency	127.750 MHz
PN Chip Rate	102.4 MHz
Data Rate	300 BPS
Data Generator	Short
C/N ₀	42 or 82 dB

The test setup for the range rate measurement performance tests is shown in figure 5-8. Table 5-12 shows the results for RMS range rate error performance using ten-1 second samples.

Table 5-12. RMS Range Rate Error Performance

RCVR No.	Signal/Noise (C/N ₀)	RMS Jitter (Hz)
1	42 dB	.004859
	82	.004923
2	42	.007762
	82	.003500

SECTION VI

CONCLUSIONS

6.1 SUMMARY

This report contains a description of the Multimode Transponder and its associated ground support and test equipment. Candidate modes of operation considered for use in an eventual tracking and data relay system servicing low data rate users were implemented in this design. System trade-off studies during Phase I identified the foreseeable technical problems of the eventual TDRSS user and the solutions to these problems were implemented in the Multimode Transponder design during Phase II.

The functional capability of the Multimode Transponder is substantial and fairly complex. The functions of: (1) command data reception, (2) telemetry data transmission, (3) full duplex voice operation, and (4) coherent range and range-rate transponding are performed in two principal modes: conventional PSK and pseudonoise. Within these modes there is a multiplicity of: (1) selectable data rates, (2) PN rates, and (3) receive and transmit frequencies. Diversity reception is provided for all modes of operation.

A striking aspect of this baseline design is its relative simplicity in light of the many TDRSS requirements. Rather than implementing each mode of operation with distinct circuitry, means were found to utilize common circuitry for all modes. The design was devised with reliability considerations in mind. For example, the duality required for diversity is done in such a way that it also represents redundancy for reliability. Should one channel of diversity fail, the transponder can still function with only minor losses in performance.

Accessibility is also a feature of the MMT/MTAR equipment design. Any PC card can be extended from its normal position to provide monitoring access to virtually any signal in the system during operation. A substantial number of test signals and all data and voice signals have been brought out to a connector in the front panel of the signal processor for easy access to/from test equipment.

The equipment can be conveniently relocated for a variety of experiments. A readily available power source of 115 VAC, single phase is all that is required for prime power. Each major assembly contains its own blowers for cooling. RF shielding has been built into the equipment so that threshold performance can be achieved with the use of a single screen room.

As the various modes of operation are compared with each other in simulated environments, the techniques best suited for the anticipated TDRSS environment will become evident. Undoubtedly problems still unforeseen, will become evident as this equipment is subjected to these environments. However, as a result of these experiments, the specifications for a transponder for future user satellites can be written with certainty.

As the TDRSS concept is refined, some of the requirements will undoubtedly change. For example, even before this equipment was delivered, it became evident that the RF frequencies for the TDRSS low data rate users would most likely be shifted to the S-band region. Fortunately the mechanical design Multimode Transponder is sufficiently flexible so that retrofits of this magnitude can be accommodated without a new chassis design. With this versatility, it is practical to modify the MMT/MTAR equipment so that valuable test data can be collected to aid in specifying the eventual TDRS user transponder requirements.

6.2 DESIGN HIGHLIGHTS

6.2.1 FLEXIBILITY

The Multimode Transponder has been designed for flexibility. All major signals are readily available from the Signal Monitor Box. All circuits can be monitored with the use of PC card extenders. All equipment operates from a standard 115 VAC, 60 Hz prime power source. All cooling air sources are self-contained. To aid in special tests, the equipment can be operated in (1) the forward mode only, (2) the return mode only, or (3) the transpond mode. The controller can be stopped at any juncture in its operational sequence to facilitate special experiments or tests.

6.2.2 PN SYNCHRONIZATION

The Multimode Transponder is a balanced system. Its acquisition threshold is equal to its tracking threshold. In other words, if the S/N ratio of an incoming PN signal is sufficient to provide the necessary data performance (data error of $\leq 10^{-5}$) the PN signal acquisition will also be achieved with good confidence at the same S/N level.

PN synchronization does not require special transmissions or preambles. Synchronization is performed on the TDRS signal even when it carries data destined for other users. Synchronization is accomplished within a few seconds (exact values dependent on signal-to-noise of either TDRS coming over the horizon or handover).

6.2.3 DOPPLER RESOLVER

A doppler resolver mechanism was implemented in the Multimode Transponder to speed up the resolvment of frequency uncertainties by a factor of 100 compared to real-time frequency search techniques. It was primarily this device which reduced the worst case acquisition time to less than 40 seconds in a PN mode of operation.

Basically, the doppler resolver (1) samples the incoming signal plus noise at the baseband, (2) performs a fast Fourier transform, and (3) identifies and verifies the presence of a signal within a particular frequency cell over the range of frequency uncertainty. The speedup is accomplished by digitally storing a signal plus noise sample and then increasing the processor clock by a factor of 100.

6.2.4 DIVERSITY COMBINING

Diversity combining was accomplished by switching to the receiver with the strongest signal. This technique was simple to implement and provided performance within 1 dB of the theoretically optimum maximum likelihood coherent combining method.

It was found that in the PN modes, the combining must be done after correlation, but prior to data detection and the development of carrier and code tracking loop error signals. The classical coherent detectors used in PN and extracted reference PSK receivers were recognized as performing the essential function of pre-detection diversity combining, so that the combining was performed with very little more than twin PN receivers.

6.2.5 MULTIPATH DISCRIMINATION

In the PN tracking modes, multipath immunity was provided for all multipath differential delays from a few microseconds up to 40 ms by suitable choice of PN sequence parameters. In the PN acquisition modes, false lock to multipath signals was prevented for differential delays up to 2 ms.

6.2.6 DATA CONDITIONING

The transponder provides for two way data transmission simultaneous with ranging or alternatively full duplex voice and ranging. Telemetry data is transmitted either uncoded or with convolutional encoding compatible with a GSFC decoder.

6.2.7 SPECIAL TEST EQUIPMENT

An MX 270B Bit Error Rate Analyzer is included with the Multimode Transponder equipment to facilitate laboratory testing. Among the functions provided are: (1) command and telemetry simulation and (2) command and telemetry message recognition and scoring.

A signal monitor box is also included for each terminal to facilitate external interface connections and signal monitoring with external test equipment.

6.3 COMPARISON OF MODULATION TECHNIQUES

Comparisons between conventional PSK and pseudonoise modulation are made in tables 6-1 and 6-2. Since many of the performance parameters do not lend themselves for comparison for both modulation techniques, the comparisons were made on the basis of advantages and disadvantages for each technique.

Table 6-1. Performance Parameters -- Conventional PSK

Advantages	Disadvantages
<ul style="list-style-type: none"> ○ Relatively simple to implement (compared to PN) ○ More reliable due to simplicity than PN ○ Less cost due to less hardware over PN ○ Theory and implementation well established ○ Optimal system in an additive Gaussian channel such as the space medium ○ Allows use of saturated amplifiers thereby giving higher system efficiency ○ Uses channel bandwidth reasonably well ○ Channelization possible to avoid interference 	<ul style="list-style-type: none"> ○ Requires coherent detection ○ Multipath sensitive ○ Attainable data quality limited by EIRP of transmitter ○ Sensitive to system phase distortion (TWT AM/PM conversion, etc., oscillator instability, etc.) ○ No inherent range and range rate

Table 6-2. Performance Parameters -- Pseudonoise Modulation

Advantages	Disadvantages
<ul style="list-style-type: none"> • Multipath rejection properties • RFI rejection properties • Available for ranging if needed • Encoding implementation trivial; decoding requires little added complexity • Still allows use of saturated amplifiers as in PSK • End to end system is transparent and so is again optimal on the space channel • Code diversity possible • Theory and implementation well established 	<ul style="list-style-type: none"> • Requires more channel bandwidth than PSK • Requires code coherence at the receiver • Requires coherent detection of data as PSK • Sensitive to system phase distortion • Data quality limited by transmitter EIRP in the thermal noise case (no RFI, multipath, etc.) • Added system cost over PSK • Catastrophic failure possible if PN can't lock-up • No channelization possible to avoid interference

6.4

FUTURE EQUIPMENT

Table 6-3 shows the anticipated equipment configuration along with estimated size and weight for a pseudonoise transponder using hardware which will be available in 1977. Full advantage would be taken of low power logic, custom hybrid circuits, and standard LSI circuits. The anticipated design would require 250 cubic inches and 25 watts of power.

Table 6-3. Size and Power — Pseudonoise Modulation
Using 1977 Technology

Assembly	Size (IN ³)	Power (Watts)
<u>RECEIVER</u>		
UHF/IF Assembly	30	0.5
RF Synthesizer	10	1.5
Local Reference/Correlator	10	0.5
Synchronous Demodulator	15	1.5
Doppler Resolver	15	2
PDM Voice	10	1
Controller	10	0.5
PN Coder/Clock/Data Processor	10	0.5
	<u>110</u>	<u>9</u>
<u>TRANSMITTER</u>		
Transmitter (37 dBm - EIRP)	100	15
Modulator/Up-Converter	10	1
Diplexer	30	-
	<u>140</u>	<u>16</u>

SECTION VII

RECOMMENDATIONS

7.1 MODIFICATIONS TO IMPROVE EXISTING EQUIPMENT

It is now evident, after integrating and testing the Multimode Transponder equipment, that some improvement in reliability and performance could be realized through equipment modification. These modifications are discussed in this section. Not only should these modifications be incorporated into the existing Multimode Transponder equipment, but they should be considered for inclusion into future TDRSS User Satellite equipment.

7.1.1 BASEBAND DATA FILTERING

Presently, baseband data is extracted from the RC filtered I channel of the Costas demodulator and subsequently processed in a "integrate and dump" filter. Much of the advantage of the "integrate and dump" filter is lost due to prior filtering in the RC filter of the Costas loop whose corner frequency is set at the data rate to minimize 3rd multiplier loss. Unfortunately, the data cannot be extracted from the I channel prior to RC filtering because the "integrate and dump" filter cannot practically accommodate the large S+N dynamics inherent at threshold for low data rates. The solution (at the cost of additional hardware) is to provide a separate RC filter for I channel data with corner frequencies set at 3X the data rate for data processing.

7.1.2 DIVERSITY COMBINER

Diversity receiver selection is currently made on the basis of relative S/N ratio. The relative goodness of the two channels is measured by comparing AGC voltages. Unfortunately, the AGC time constants are slow and phase lock of one of the receivers may go unnoticed for several seconds during acquisition. As a result,

acquisition performance is degraded. The condition of phase lock (K) should be included in the selection decision to remedy this problem. Channel selection should be based on the following conditions:

Channel No. 1

(Sel 1) $(K_1 + \overline{K}_2)$

Channel No. 2

(Sel 2) $(K_2 + \overline{K}_1)$

7.1.3 PN REACQUISITION

After a PN tracking mode has been established and then a loss of lock condition occurs, a PN autosearch sequence is initiated. During this time, the PN code is advanced and retarded in time over a ± 16 PN chip interval. If a false alarm occurs during this time, the autosearch cycle is aborted with no further opportunity for reacquisition. The equipment should be modified so that the PN autosearch sequence is continued unless sync is verified by (K) from either channel.

7.1.4 DOPPLER RESOLVER

In future equipment the doppler resolver resolution should be doubled. At near threshold conditions, the doppler resolver will locate an incoming signal to within ± 1 window and may consequently offset the center frequency of the VCO by as much as the data rate. This amount of offset reduces the probability of acquisition substantially. If the frequency uncertainty could be reduced to $1/2$ the data rate, acquisition performance would be substantially improved.

The performance of the doppler resolver could also be improved by allowing more than one "fine doppler" correction. In some cases a single "fine doppler" correction does not place the VCO frequency to within the acquisition range of the phase locked loop due to nonlinearities within the loop.

7.1.5 DEMODULATOR APERTURE

The S+N aperture of the synchronous demodulator was designed to be adequate for threshold conditions defined by data error rates of 1×10^{-5} ($E_b/N_0 = 10$ dB). In future equipment, this aperture should be extended to allow carrier tracking several dB below this threshold.

7.2 S-BAND MODIFICATION

Since it is likely that low data rate users will operate at S-band frequencies instead of UHF frequencies according to the current concept of the TDRSS, it is recommended that the multimode transponder be modified to operate back-to-back at S-band. The results of testing the modified equipment have considerable merit for the following reasons:

- Theoretical performance calculations could be verified with real hardware.
- A baseline of performance for PN versus PSK could be established.
- PN modulation techniques could be evaluated to verify:
 - Rapid PN synchronization
 - PN ranging
 - Diversity reception of PN signals
 - Digitized voice performance
- Multipath rejection properties of PN could be evaluated.
- Implementation of the first coherent PN user transponder could be verified at S-band.

7.3 LAB TEST PROGRAM

Since the Multimode Transponder design is complete and ready for testing, laboratory testing of the PN techniques, data rates, coherent transponding techniques, polarization diversity techniques, etc., could yield substantial insight into candidate modes of operation for a future user transponder in a relatively short period of time and at nominal cost. As test conductor for the experiments, MRL would:

- Provide the engineering personnel for all test and evaluation.
- Serve as an M&O station and provide for all maintenance and overhaul of the multimode transponder equipment during the experiments.
- Collate this data into a useful format.
- Provide summaries and performance reviews suitable for presentation to management.